Editorial

It is our great pleasure to present the first issue of ACM JETC, the ACM Journal on Emerging Technologies in Computing Systems. The economic and technical challenges impeding the continued scaling of semiconductor technology has resulted in the search for alternate mechanical, biological/biochemical, nanoscale electronic, and quantum computing and sensor technologies. As the underlying nanotechnologies continue to evolve in the labs of chemists, physicists, and biologists, it has become imperative for computer scientists and engineers to translate the potential of the basic building blocks (analogous to the transistor) emerging from these labs into information systems.

ACM's new Journal on Emerging Technologies in Computing Systems (JETC) will provide comprehensive coverage of innovative work in the specification, design analysis, simulation, verification, testing, and evaluation of computing, communication and sensing systems constructed out of emerging technologies and advanced semiconductors (including nano-scale CMOS systems). Topics within the scope of JETC will include:

- logic primitive design and synthesis—how to design computational logic primitives from the new nanotechnologies and design tools supporting their effective design and verification;
- system-level specification, design and synthesis—how to interconnect these computational primitives to build complete information systems, and design tools for specifying, synthesizing, and verifying such systems;
- software-level specification, design and synthesis—how to develop the necessary software so that applications can be effectively mapped onto information systems implemented using these new nanotechnologies and tools for generating and verifying the software; and
- mixed-technology systems—how to interface across potentially hybrid nanotechnologies that may co-exist in the same information system.

JETC will publish research papers (approximately 20 double spaced pages, 10 point font), tutorial and survey papers (approximately 40 to 50 double spaced pages, 10 point font with an extensive bibliography), and short technical notes (less than ten pages). ACM JETC will be published quarterly, and each issue will contain approximately three to four papers.

We have assembled a truly outstanding editorial board representing diverse emerging technology fields such as nano-scale CMOS, quantum computing, molecular computing, and biochips. A brief biography of the associate editors is provided in this issue to highlight the technical focus areas covered by the TECS editorial board.

The first issue includes two papers. The first paper provides a tutorial covering imminent challenges facing designers using nanoscale CMOS technology. The second paper proposes a partitioning and placement algorithm for automatic Quantum Dot Cellular Architecture layout. We hope that readers will enjoy this issue. We look forward to your submissions and help with the

review process. Please visit us at <http://www.cse.psu.edu/~mdl/jetc/> for more information.

MARY JANE IRWIN
Co-Editor-in-Chief
 VIJAYKRISHNAN NARAYANAN
Co-Editor-in-Chief

Editorial Board

Mary Jane Irwin has been on the faculty at Penn State since 1977 where she currently holds the title of the A. Robert Noll Chair in Engineering in the Department of Computer Science and Engineering. Her research and teaching interests include computer architecture, embedded and mobile computing systems design, power aware design, and electronic design automation. Dr. Irwin received her Ph.D. degree in computer science from the University of Illinois in 1977. She received an Honorary Doctorate from Chalmers University, Sweden, in 1997 and the Penn State Engineering Society's Premier Research Award in 2001. She was named a Fellow of The Institute of Electrical and

Electronic Engineers (IEEE) in 1995, a Fellow of The Association for Computing Machinery (ACM) in 1996, and was elected to the National Academy of Engineering (NAE) in 2003.

Vijaykrishnan Narayanan is an associate professor of Computer Science and Engineering at the Pennsylvania State University. His research interests are in the areas of energy-aware reliable systems, embedded Java, nano/VLSI systems, and computer architecture. Dr. Narayanan has received several awards including the IEEE CAS VLSI Transactions Best Paper Award in 2002, the Penn State CSE Faculty Teaching Award in 2002, the NSF CAREER Award in 2001, the ACM

SIGDA outstanding new faculty award in 2000, Upsilon Pi Epsilon award for academic excellence in 1997, the IEEE Computer Society Richard E. Merwin Award in 1996, and the University of Madras first rank in Computer Science and Engineering in 1993. Dr. Narayanan serves on the steering committee of the IEEE Computer Society Annual Symposium on VLSI and has been serving on the executive committee of the International Symposium on Low Power

Electronics and Design since 2001. He also serves as an associate editor for the IEEE Transactions on VLSI and the Journal of Low Power Electronics.

Luca Benini is an Associate Professor at the Department of Electrical Engineering and Computer Science (DEIS) of the University of Bologna. Dr. Benini's research interests are in innovative hardware architectures and hardware-software systems, with special emphasis on ambient intelligence, energy-efficient applications. On these topics he has published more than 250 papers in international journals and conferences and three books. He has been program chair and vice-chair of Design, Automation and Test in Europe Conference. He has been a member of the technical program committee and organizing committee of several technical conferences, including the Design Automation Conference, International Symposium on Low Power Design, and the Symposium on Hardware-Software Codesign. He is a senior member of the IEEE.

Fred Chong is an Associate Professor and Chancellor's Fellow in the Department of Computer Science at the University of California at Davis. He received his Ph.D. from MIT and is a recipient of the National Science Foundation's CAREER award. His current research focuses on novel computing technologies, secure and reliable systems, and next-generation embedded and sensor architectures.

Krishnendu Chakrabarty received a Bachelor of Technology degree from the Indian Institute of Technology, Kharagpur, in 1990, and his M.S.E. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1992 and 1995, respectively, all in Computer Science and Engineering. He is now an Associate Professor of Electrical and Computer Engineering at Duke University. Dr Chakrabarty is a recipient of the National Science Foundation Early Faculty (CAREER) award and the Office of Naval Research Young Investigator award. His current research projects include: testing of integrated circuits; embedded real-time systems;

distributed sensor networks; microfluidics-based biochips. He is a recipient of a best paper award in 2001 at the Design, Automation and Test in Europe Conference. He is also a recipient of the Humboldt Research Fellowship, awarded by the Alexander von Humboldt Foundation, Germany. Dr Chakrabarty serves as an Associate Editor of IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems and as an Editor of the Journal of Electronic Testing: Theory and Applications. He is a senior member of IEEE and a member of ACM.

Vivek De is a Senior Principal Engineer and Manager of Low Power Circuit Technology research at Intel's Microprocessor Technology Labs in Hillsboro, Oregon. He received his Ph.D. in Electrical Engineering from Rensselaer Polytechnic Institute, Troy, New York in 1992. He has authored 122 technical papers in refereed international conferences and journals, and 4 book chapters on low power circuits. He has 75 patents granted and 74 more patents filed (pending) in the areas of low-power and high-performance

circuits and devices. He is the recipient of a best paper award at the 1996 IEEE International ASIC Conference in Portland, Oregon for his work on the GENESYS system simulator. He served as general chair of the 2002 ACM/IEEE International Symposium of Low Power Electronics & Design (ISLPED'02), technical program chair of ISLPED'01, and the 2002 Great Lakes Symposium on VLSI (GLSVLSI'02), and technical program vice-chair of the 2002 IEEE International Symposium on Quality Electronics Design (ISQED'02). He served as the guest editor of a special issue of IEEE Transactions on VLSI Systems on low power.

Paul D. Franzon is currently a Distinguished Alumni Professor of Electrical and Computer Engineering at North Carolina State University. He earned his Ph.D. from the University of Adelaide, Adelaide, Australia in 1988. He has also worked at AT&T Bell Laboratories, DSTO Australia, Australia Telecom, and two companies he cofounded, Communica and Light-Spin Technologies. His current interests center on the technology and design of complex systems incorporating VLSI, MEMS, advanced packaging, and molecular electronics. Application areas currently being explored include novel advanced packaging structures, Network Processors, SOI baseband radio circuit

design for deep space, on-chip inductor and inductance issues, RF MEMS, and moleware circuits and characterization. He has led several major efforts

and published over 120 papers in these areas. In 1993, he received an NSF Young Investigators Award, in 2001 was selected to join the NCSU Academy of Outstanding Teachers, and in 2003, selected as a Distinguished Alumni Professor.

José A.B. Fortes received his Ph.D. degree in Electrical Engineering from the University of Southern California. From 1984 until 2001, he was on the faculty of the School of Electrical Engineering of Purdue University at West Lafayette, Indiana. In 2001, he joined both the Department of Electrical and Computer Engineering and the Department of Computer and Information Science and Engineering of the University of Florida as Professor and Bell-South Eminent Scholar. From July 1989 through July 1990, he served at the National Science Foundation as director of the Microelectronics Systems Architecture program. His research interests are in the areas of nanocomputing, computer architecture, distributed computing, and fault-tolerant computing. He has authored or co-authored over 100 technical papers. His research has been funded by the National Science Foundation, the Office of Naval Research, AT&T Foundation, IBM, General Electric, NASA, and the Semiconductor Research Corporation. José Fortes is a Fellow of the Institute of Electrical and Electronics Engineers (IEEE) professional society. He is on the Editorial Boards of IEEE Transactions on Parallel and Distributed Systems; ACM Journal on Emerging Technologies in Computer Systems; Cluster Computing: The Journal of Networks, Software Tools and Applications; the International Journal on Parallel Programming; and the Journal of VLSI Signal Processing.

Dr. Seth Copen Goldstein received his Ph.D. in Computer Science at the University of California at Berkeley in 1997. His undergraduate work was undertaken at Princeton University in the Department of Electrical Engineering and Computer Science. Currently Dr. Goldstein is an Associate Professor in the School of Computer Science at Carnegie Mellon University. Before attending UC Berkeley, Seth was CEO and founder of Complete Computer Corporation which developed and marketed object-oriented programming tools. His research focuses broadly on using nanotechnology in computer science. He is involved in two main efforts, the first, Phoenix, involves compilers and architectures for novel computing systems with a focus on reconfigurable computing. His second effort, Claytronics, involves realizing programmable matter.

Dr. Kogge received his Ph.D in EE from Stanford in 1973. From 1968 until 1994, he was with IBM's Federal Systems Division and was appointed an IBM Fellow in 1993. In August 1994, he joined the University of Notre Dame as first holder of the McCourtney Chair in Computer Science and Engineering. He is currently the Associate Dean for Research, College of Engineering. He is also an IEEE Fellow and a Distinguished Visiting Scientist at JPL. He holds over 20 patents

and is author of two books, including the first text on the now ubiquitous technique of hardware pipelining. His current research areas include massively parallel processing architectures, advanced VLSI and nano technologies, and non-von Neumann models of programming and execution. Major current projects include merging logic and memory on the same chip, inherently low power computer architectures, and the use of nano-level technologies such as Quantum dot Cellular Automata.