Editorial: Special Issue on 3D Integrated Circuits and Microarchitectures

This special issue of the *ACM Journal of Emerging Technologies in Computing Systems* is dedicated to three-dimensional integrated circuits and microarchitectures. Three-dimensional (3D) Integrated Circuits have emerged as an attractive option for overcoming the barriers in interconnect scaling. To efficiently exploit the benefits of 3D technologies, design techniques and methodologies for supporting 3D designs are imperative; design space exploration at the architectural level is also essential to fully take advantage of the 3D integration technologies and build a high performance chip.

A call for papers for the JETC special issue was announced in August 2007. All submissions went through the regular review process of JETC. After review and appropriate revisions, five papers on diverse topics related to 3D integration were accepted for the special issue.

In the first article of this special issue, Kgil et al. describe a new architecture design called PicoServer, which employs 3D technology to bond Chip-Multiprocessors (CMPs) die to multiple DRAM memory dies sufficient for a primary memory. The use of 3D stacks facilitates wide low-latency buses between processors and memory and removes the need for L2 caches. Such architecture enables the design of compact and energy efficient servers. The second article by Ma et al. explores fine-granularity 3D integration and its impact on the microarchitecture design. The authors study the multilayer block implementation alternatives and propose a microarchitecture-physical codesign framework to perform thermal-aware cooptimization of microarchitecture design and physical design. It also demonstrates that thermal-aware design planning and the use of thermal vias can help mitigate the temperature increases due to vertical integration. The third article by Zhan and Sapatnekar presents a design automation solution for power delivery in 3D IC. A partition-based algorithm is proposed to assign modules to different Vdd domains in a two-level stacked-Vdd circuit. In the fourth article, Ferri et al. study the impact of process variations on the performance and parametric yield of 3D ICs and provide integration strategies that maximize the parametric yield. Finally, in the fifth article, Miyakawa et al. present a 3D stacking technology developed by Honda Research Institute. The process steps for this wafer-to-wafer stacking method are described in detail. A prototype of a 3-layer stacking chip is fabricated using 0.18 μ m CMOS technology based on 8-inch wafers. The 3-layer prototype chip consists of a microprocessor layer, a memory layer, and a custom logic layer.

We would like to thank all the authors who responded to the call for papers and the reviewers who provided detailed and insightful reviews in a timely

manner. We also thank the Editor-in-Chief and the editorial staff for the help on putting together this special issue. We hope that this special issue can stimulate further research in a young and exciting area of three-dimensional integrated circuits and microarchitecture designs.

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