Editorial to Special Section on Networks on Chip: Architecture, Tools, and Methodologies

Continuous technology scaling has enabled the integration of hundreds of processing cores on the same silicon substrate, therefore allowing for the concurrent execution of multiple applications on a chip. For such systems, traditional solutions for on-chip communication are likely unable to scale, thereby requiring a departure from classic on-chip communication paradigms. The Networks-on-Chip (NoC) approach has emerged as the most promising communication paradigm for massively integrated multicore systems. To disseminate some of the best research outcomes in this field, in 2012 the *ACM Transactions on Design Automation of Electronic Systems* released a solicitation for this special section NOC-ATM: Networks on Chip: Architecture, Tools, and Methodologies. Nineteen submissions were received of which five articles of excellent quality were selected for publication through a rigorous review process. This special section reports on recent advances in development of on-chip communication technology, architecture, design methods and applications while bridging work in related research communities, including computer architecture, networking, circuits and systems, embedded systems, and design automation.

Addressing the importance of dynamic power management in NoC systems, “Dynamic Power Management for Multidomain Systems-on-Chip Platforms: An Optimal Control Approach” by Paul Bogdan, Radu Marculescu, and Siddharth Jain proposes a novel workload modeling approach that extracts fractal behavior of real applications. Not only is the approach completely feasible and efficient to perform online, but it also enables a constrained finite horizon fractional control approach for optimizing total power consumption under isoperformance conditions. The newly proposed optimal control approach achieves 70% power savings and outperforms other classic schemes based on PID and LQR control by a factor of 2X. The methodology is scalable to many-core systems and allows for fast convergence in achieving true optimal power consumption under highly variable workloads.

In the same vein of NoC power management, but now addressing the issue of last level caches (LLC), the second article, entitled “In-Network Monitoring and Control Policy for DVFS of CMP Networks-on-Chip and Last Level Caches” by Xi Chen, Zheng Xu, Hyungjun Kim, Paul Gratz, Jiang Hu, Michael Kishinevsky, and Umit Ogras, employs dynamic voltage and frequency scaling (DVFS) policies for NoC shared, distributed LLC. Achieving true dynamic power management via DVFS is more difficult than classic individual link/core-based DVFS since it involves spatially distributed monitoring and control. To alleviate these challenges, the authors propose an average memory access time (AMAT)-based monitoring technique in conjunction with DVFS based on PID control theory, which achieves a 27% energy savings with little performance drop.

The third article, entitled “Adaptive Virtual Channel Partitioning for Network-on-Chip in Heterogeneous Architectures” by Jaekyu Lee, Si Li, Hyesoon Kim, and Sudhakar Yalamanchili, addresses the issue of how to efficiently share on-chip resources between cores for the heterogeneous system, in particular the on-chip network. The authors propose a feedback-directed virtual channel partitioning (VCP) mechanism for on-chip routers to effectively share network bandwidth between CPU and GPU cores in a heterogeneous architecture. The proposed mechanism balances on-chip network bandwidth for applications running on CPU and GPU cores by

choosing the best partitioning configuration in an adaptive manner and improving system throughput by 15% across 40 heterogeneous workloads.

Moving down the system stack, the fourth article, “Ordering Circuit Establishment in Multiplane NoCs” by Ahmed Abousamra, Alex Jones, and Rami Melhem, describes a hybrid packet/circuit switched multiplane network optimized to reduce latency in order to improve system performance and/or reduce system energy. By enforcing the order in which resources are scheduled and utilized rather than a fixed time, the NoC can take advantage of messages that arrive early, while naturally tolerating message delays due to contention. In simulations of 16- and 64-core CMPs, average NoC energy savings of 43% and 53% are achieved, respectively. Furthermore, circuits are proactively reserved for a return data message as a request message traverses the NoC. Results show a speedup in execution time of up to 16%, with an average of 10%, over a purely packet-switched NoC.

Finally, the article entitled “Deflection Routing in 3D Network-on-Chip with Limited Vertical Bandwidth” by Jinho Lee, Dongwoo Lee, Sunwook Kim, and Kiyoun Choi proposes a deflection routing scheme for 3D NoC with serialized TSVs for vertical links. In a 3D system architecture, deflection routing can yield better performance than buffered routing, but state-of-the-art approaches cannot be directly applied because serialized TSV links take longer to send data than ordinary planar links. This article proposes a method to mitigate this effect and solve resulting deadlock and livelock problems. Compared to simple buffered routers, the proposed approach performs 43.3% faster and consumes 63.0% lower energy for typical on-chip traffic. On real application benchmarks, it performs 11.0% faster than a buffered router with four virtual channels, consumes 82.2% lower energy consumption, and exhibits 6.32 times better energy efficiency.

The guest editors would like to thank all of the reviewers for their valuable contributions in the review process. Only through their critical comments and feedback and the support of the Editor-in-Chief, Massoud Pedram, has it been possible to assemble this high-quality special section. The selected articles cover novel approaches and techniques addressing challenging issues in NoC systems at various levels of abstraction, which we hope the readers will find intellectually satisfying, while also opening new directions in NoC system modeling, analysis, and optimization.

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