Guest Editorial: Special Issue on Emerging Technologies in Embedded Software and Systems

The design and development of embedded software and systems is evolving rapidly in recent years. This is partially due to the advanced communication techniques and processor technologies (e.g., multicores) as well as the evolution of new application domains, such as Cyber-Physical Systems (CPS) and Internet of Things (IoTs).

Embedded systems now influence more areas of our daily life, from smart appliances to automotive and public transportation infrastructure. These new applications bring increased complexity in functional requirements and demand close-interaction between embedded systems, their users and the surrounding environment. These requirements and demands pose a new set of challenges (such as safety, security and adaptivity) for the effective and efficient design and development of embedded software and systems.

This special issue, entitled “Emerging Technologies in Embedded Software and Systems,” tackles these challenges by exploring novel and bold ideas of emerging technologies for the next generation embedded software and systems. Together with an open call soliciting novel contributions, selected top papers from the 2015 IEEE International Conference on Embedded Software and Systems (ICESS) were invited, which leads to a total of 41 submissions. This allows us to selected 10 high-quality articles. We hope you will find them interesting and enjoy reading them.

The first article, “HYPNOS: An Ultra-Low-Power Sleep Mode with SRAM Data Retention for Embedded Micro-Controllers,” by Hrishikesh Jayakumar, Arnab Raha, and Vijay Raghunathan, studies a new ultra-low-power sleep mode for micro-controllers in heavily duty-cycled embedded systems, which can decrease the power consumption in sleep mode. Here, energy consumption can be reduced by as much as 6.45x.

The second article, “Reducing Power Consumption and Latency in Mobile Devices Using an Event Stream Model,” by Stephen Marz and Brad V. Zanden, develops an efficient Event Stream Model (ESM), which is a push model that allows a process to sleep as long as no event occurs, but then immediately awakens a process when an event occurs. It eliminates the polling loop, and thus reduces unnecessary power consumption.

The third article, “Image-Content-Aware I/O Optimization for Mobile Virtualization”, by Renhai Chen, Yi Wang, Jingtong Hu, Duo Liu, and Zili Shao, studies a novel I/O optimization technique for mobile virtualization by identifying the metadata of a guest file system and storing them in a small additional NVM (Non-Volatile Memory), which is faster and more endurable.

The fourth article, “Cache-Partitioned Preemption Threshold Scheduling,” by Zonghua Gu, Chao Wang, and Haibo Zeng, studies the integration of cache partitioning and preemption threshold scheduling to optimize schedulability for both Fixed-Priority and Earliest Deadline First scheduling algorithms on a uniprocessor system. Each subset of tasks assigned the same cache partition is considered as a nonpreemptive group with the same preemption threshold to eliminatethe cache-related preemption over-heads.

The fifth article, “Adaptive Workload Management in Mixed-Criticality Systems,” by Biao Hu, Kai Huang, Gang Chen, Long Cheng, and Alois Knoll, investigates how to

adaptively manage the low-critical workload during runtime to maximize their services while meeting the timing constraints of high-critical tasks for mixed-criticality systems.

The sixth article, “Automatic Parallelization of Multi-Rate Block Diagrams of Control Systems on Multi-Core Platforms,” by Cumhuri Tuncali, Georgios Fainekos, and Yann-Hang Lee, considers the problem of parallelizing model block diagrams for real-time embedded applications on multi-core architectures. It presents a Mixed Integer Linear Programming (MILP) formulation to find a feasible mapping of the blocks to different CPU cores. Both single-rate and multi-rate models are considered.

The seventh article, “Crosstalk-Aware Automated Mapping for Optical Networks-on-Chip,” by Edoardo Fusella and Alessandro Cilardo, studies optical Networks-on-Chip, which provides a promising answer to address the increasing requirements of ultra-high bandwidth and extremely low power consumption. Several algorithms are proposed, which automatically map the application tasks onto a generic mesh-based photonic NoC architecture such that the worst-case crosstalk is minimized.

The eighth article, “GPUrpc: Exploring Transparent Access to Remote GPUs,” by Yuki Iida, Yusuke Fujii, Takuya Azumi, Nobuhiko Nishio, and Kato Shinpei, presents GPUrpc, a remote procedure call (RPC) extension to Gdev, which allows developers to use CUDA for GPGPU development work to achieve first-class GPU resource management. Here, to reduce communication overhead, GPUrpc explores an RPC based on a low-level API than CUDA that does not require communication for efficiency.

The ninth article, “Game Theory-Based Active Defense for Intrusion Detection in Cyber-Physical Embedded Systems,” by Kun Wang, Miao Du, Dejun Yang, Chunsheng Zhu, and Yan Zhang, proposes a new attack-defense game model to detect malicious nodes using a repeated game approach for Embedded Sensor Networks (ESNs), which have limited power, storage, and processing capabilities where existing security mechanisms for wired or wireless networks cannot be applied directly. Error detection and missing detection are taken into consideration in Intrusion Detection Systems (IDSs) where a game tree model is introduced to solve this problem. In addition, they analyze and prove the existence of pure Nash equilibrium and mixed Nash equilibrium.

The tenth article, “ScorePlus: A Software-Hardware Hybrid and Federated Experiment Environment for Smart Grid,” by Song Tan, Wen-Zhan Song, Steve Yothment, Junjie Yang, and Lang Tong, studies a federated experiment environment for Smart Grid, which can enable multiple software emulators and hardware testbeds at different locations connect and form a unified Smart Grid system. ScorePlus can run as a resource plugin in OpenStack cloud computing platform.

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