Neuromorphic 3D Integrated Circuit: A Hybrid, Reliable and Energy Efficient Approach for Next Generation Computing

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ABSTRACT

In this paper, we proposed to use 3D integration technology to create a neuromorphic hardware system that is compatible with current technology, provides high system speed, high density, massively parallel processing, low power consumption, and small footprint. The Through Silicon Vias (TSVs) used in the 3D neuromorphic structure provide high density integration and energy efficient links for transferring information through multiple neuron layers. This work details how a 3D neuromorphic system is benefited from the redundant TSV with substantial design-area reduction. We discussed the yield and reliability issues and explained the impact in neuromorphic 3D system design. A spiking neuron model is developed for the proposed 3D system. Furthermore, a new methodology have been proposed by introducing oxide around the bump that could significantly enhance the TSV capacitance in 3D Neuromorphic Computing (NC) system.

Keywords

Neuromorphic computing; 3D integration; TSV; Yield; Reliability; Spiking neuron.

1. INTRODUCTION

With the increasing demand of high performance computing system, neuromorphic computing gains significant momentum and spurs the brain-inspired computing hardware development. Such systems could offer biological perception and process cognitive information efficiently within a very compact platform without being constrained by the scaling issues of conventional Complementary metal-oxide-semiconductor (CMOS) technologies [1]. Neuromorphic computing system containing 100 million “neurons” with 1 trillion “synaptic connections” have been projected within the near future [2]. Such systems will require high complexity, high connectivity, and massively parallel processing to accomplish increasingly demanding computational tasks [2]. Traditional two-dimensional (2D) integration will be incapable of meeting these requirements. Hence, three-dimensional (3D) integrated circuit (ICs) is very advantageous for neuromorphic computing which offer a promising near-term solution for pushing beyond Moore’s Law [3].

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Having excellent scalability, and compatibility with current technology, 3D IC successfully overcome the limitation of 2D neuromorphic IC [4]. Applying 3D integration to neuromorphic computing will offer the following benefits:

- ❑ Provide high complexity, connectivity, and massively parallel processing circuitual system for highly demanding computational task.
- ❑ Bandwidth limitation, higher routing cost, larger occupied area by 2D circuits [5] can be resolved by incorporating 3D IC technology with the neuromorphic hardware system.
- ❑ 3D interconnections offer very fast and energy efficient links [6] that make excellent distribution and communication among the neuron layers.

In neuromorphic computing, high density membrane capacitor plays a key role in the synaptic signaling process, especially in a spike firing analog implementation of neurons. Membrane capacitance generally occupies a significant portion of the design area of neuromorphic chips. Since redundant and dummy TSVs constitute a significant fraction of the total TSVs, we can make them more “useful” by configuring them to serve as membrane capacitors. However, the complicated process technology and fabrication methodology of TSV based 3D IC introduces significant yield and reliability challenges. Due to the fault occurs during the manufacturing process and failures during the execution-time, these issues appear and significantly affects the performance of the system. The yield of a 3D IC mainly depends on the process variation, defects, and changing the physical structures of TSV/dies and their bonding. Whereas, the reliability comes from the associated thermal issues and fabrication process. Therefore, it is very important to study the yield and reliability assessment demonstration in neuromorphic 3D IC.

This work details how a 3D neuromorphic system can be implemented with a virtual neuronal membrane that included TSV interconnects. In this paper, we propose a novel 3D neuromorphic computing architecture by exploring TSV configurations to adapt them for use as capacitors. We discussed how our proposed methodology does not degrade yield and reliability, but gets benefit from the overall system architecture. Besides, we come up with a new method to enhance the TSV capacitance to serve as necessary membrane capacitance.

2. 3D NEUROMORPHIC COMPUTING SYSTEM

In this section, the necessity of 3D integration in neuromorphic computing, proposed 3D neuromorphic structure, TSVs as membrane capacitance in 3D NC IC, yield and reliability issues of neuromorphic 3D structure are illustrated.

2.1 Necessity of 3D Integration in NC

In order to realize the true potential of neuromorphic computing in VLSI technology, the application of analog, digital, and mixed-signal IC based neural chips has been explored and fabricated. To

reproduce the biophysical process, there are some potential neural chips like TrueNorth chip: IBM, Neurogrid chip: Stanford University, and BrainScales project by EU FET HBP has been developed [7]. Table 1 describes the total number of neurocores, neurons, and synapses of these neuromorphic chips.

Table 1. Large scale neuromorphic chip implementation

Neuromorphic Chip	BrainScales	NeuroGrid	TrueNorth
Neurons	200K/wafer	1 million	1 million
Synapses	5300/wafer	>1 billion	256 million
Neurocores	-	16	4096

However, all of these neuromorphic chips are fabricated using 2D technology while some insurmountable obstacles are introduced by 2D planar circuitry like bandwidth problem, with larger area etc. Figure 1 shows the die photo and layout of a neuron in TrueNorth chip. The scalability and higher routing cost are the paramount factors in these 2D chips and very challenging to overcome.

Figure 1. TrueNorth Chip (a) Die Photo (b) Physical layout of single core [8]

Applying 3D interconnection in neuromorphic system, all the issues can be resolved and it becomes possible to get excellent distribution and communication among the neuron layers. The massive parallelism provides main contribution to estimate the performance of human brain. Therefore, the fast massively parallel processing in biological neural systems can be utilized for the high speed computation with low energy cost. In neuromorphic 3D IC, synaptic crossbars are being used that provides high density interconnection with greater reduction in parasitic. In particular, these are regarded as promising solution for modeling key features of biological synapses due to their nano scale dimensions, capacity to store multiple bits of information per element and low energy requirement to write distinct states. Physically well connected synapses can enhance the performance of neural network which naturally makes the necessity of 3D integration technology in neuromorphic computing.

2.2 Novel Neuromorphic 3D IC Structure

3D neuromorphic device is mounted on a semiconductor substrate and each chip in the 3D structure represents a functional unit. In a neuromorphic device, neurons are represented by CMOS substrate, while axons and dendrites are implemented by nanowires, and synapses denotes the junctions of crossing wires. As illustrated in Figure 2, the 3D neuromorphic structure contains different cell layers that include High speed buses, CMOL Crossnet, CMOS substrate, membrane capacitance, nano devices, and bipolar spin neurons. This neuromorphic electronic architecture of brain and retina can be fabricated by using CMOS IC that contains a great number of microcircuit and TSV interconnects. TSVs offer a great deal of benefits in a neuromorphic 3D IC as it adds all the features of vertical stacking of conventional 3D IC.

Figure 2. Proposed TSV based 3D neuromorphic IC

2.3 TSV in 3D NC IC

Neuromorphic system introduces huge capacitance for the storage of internal information. In general, neuron capacitance occupies a significant portion of the design area of neuromorphic chips. Figure 3 (a) and 3 (b) represents the layout of a single neuron using 90nm and 130nm CMOS technology respectively where in both cases the capacitor consumes a large portion of the neuron's design area.

Figure 3. Capacitor (yellow) in neuron chip (a) 90nm CMOS [9] (b) Layout, 130nm CMOS [10]

In the current state-of-the-art of neuromorphic IC design, it has been found that, most of the analog and mixed signal neuron design requires larger capacitors which occupies a notable area of the chip. In these design methodology, the capacitors occupy from 25% to 75% of the total design area while their values vary from 40 fF to 1.1 pF [11-13]. According to the International Technology Roadmap for Semiconductors (ITRS), the current CMOS technology of capacitance 5-7 fF/μm² need to be increased up to 13 fF/μm² by next 5 years. This slow increase presents a huge density-scaling challenge for conventional MOS capacitors. Hence, the unused TSVs in 3D neuromorphic chip are promising candidate that could provide the alternative route to achieve high density capacitance.

Among different capacitances of neuromorphic chip, membrane capacitance plays a key role for the implementation of spiking neuron. It is the stored charge of ions across either side of cell that results from the membrane composition of bilayer phospholipids. The cell membrane serves as an insulating dielectric between the intracellular and extracellular fluid with opposite polarity ions at either side. This disequilibrium ionic charge on each side of the

membrane generates potential difference which forms the membrane capacitance and these are illustrated in Figure 4.

Figure 4. Structure of the cell membrane of a neuron

This capacitance often used as a measure of the changes to membrane surface area and therefore, the total membrane capacitance is directly proportional to surface area and the dielectric properties of membrane. However, TSVs in 3DIC is composed of metal conductor lined with insulator dielectric and buried in silicon substrate and similar to the MOS structure shown in Figure 5(a). Depending on the substrate doping and voltage condition, a capacitance is formed between the metal and substrate in different regions like accumulation, depletion, and inversion.

Figure 5. TSVs as capacitance (a) Cross-section top view (b) Neuromorphic structure [5]

This TSV capacitance can be used as membrane capacitance and all the unused TSVs can be perfectly utilized by producing capacitance in an energy efficient hardware analog neuron design. The architecture of utilizing the unused TSVs as membrane capacitance is shown in Fig. 5(b) where the active TSVs can also be used as interconnects to transmit signals. It has been found that a single TSV with $38.5 \mu\text{m}^2$ footprint can offer capacitance of 550fF which is equal to $91.7 \mu\text{m}^2$ conventional MOS capacitors [14]. Joulbert *et al* [5] provides some example of neuron connectivity where it has been found that the TSV can vertically connect neuron blocks and can be used as capacitive elements.

2.4 Yield Issue in the Proposed Design

The yield in 3D neuromorphic IC depends on die yield, TSV Yield, and the bonding yield and this is illustrated in Figure 6. These yields are mainly affected by the process variation and changing the physical structure of dies/TSVs. The process variation and optimization are the key issues that causes Cu extrusion and hence the TSV parasitic characteristics are changed. Besides this, misalignment and random open defects can happen in TSV bonding and fabrication process respectively which severely impact the TSV yield.

However, the foundries impose a minimum TSV density rule to maintain the planarity of the wafer during chemical and mechanical polishing (CMP). This rule results in many dummy TSVs, for example, the 3D-MAPS processor contains 2,240 dummy TSVs

[15]. Due to the requirement of high density interconnect in neuromorphic 3D IC, these dummy TSVs are very helpful.

Figure 6. Total Yield in 3D neuromorphic IC

It has been reported that 15%–25% of all redundant TSVs in 3D chips are truly necessary [16] for the enhancement of chip yield. Therefore, the design rule naturally enhance the yield in 3D neuromorphic chip and huge amount of dummy TSVs remains left. Figure 7 shows the grouping of regular and redundant TSVs for the improvement of yield in 3D IC.

Figure 7. Grouping technique of regular and redundant TSVs [17]

By inserting new spare/ground TSVs and sharing the redundant TSVs across the neighboring die could change the yield. However, in our study we don't change the signal to ground ratio or the number of the TSVs or their physical sizes. We only need to utilize the remaining dummy TSVs which will not affect in the physical structure. Also, our introduced methodology for capacitance enhancement does not require any process change and we don't deal with these factors that affect TSV/die/bonding yield. Hence, the proposed technique in this work will not change the TSV assignment or TSV array physical structure and the yield will not be impacted negatively by this work.

2.5 Reliability in Neuromorphic 3D IC

Reliability is considered as one of the major concerns in designing 3D ICs and need to be quantified and evaluated perfectly before the real production application. Due to the imperfect fabrication process and thermal issues, the critical reliability problem occurs. Having higher density integration in traditional 3D IC, the thermal dissipation is inefficient and causes the reliability challenges. The higher thermal density accelerates the electromagnetic effect in the ultra-fine electrical path and introduced thermal induced crack in TSV and silicon substrate. These issues can be resolved by making ensure the low temperature bonding and TSV process which can reduce the thermal stress and improve the reliability. Figure 8 shows the fabricated stacked wafer with multiple TSVs where the pumping stress is reduced by lowering the TSV process temperature and the reliability is enhanced.

However, the computation in 3D neuromorphic system is inherently parallel and this massive parallelism characteristic helps to implement the lower operating clock frequency in the circuitual system without any compromise with the output. This low clock

frequency in neural system requires lower power density which is directly related to thermal issues.

Figure 8. SEM image of fabricated stacked wafers and multiple TSVs [18, 19]

Therefore, compared with traditional high frequency 3D IC, neuromorphic 3D system has the ability to reduce the thermal stress and the reliability is greatly improved.

3. SPIKING NEURON MODEL IN 3D NC IC

The spiking neuron model has become an essential key computational unit for neuronal action potential across the cell membrane. For the integration of electrical inputs of a neuron, it is necessary to estimate the membrane capacitance that determines the neuronal time constant.

The leaky integrate-and-fire (LIF) model is a formal spiking neural model stimulated by external current and describes the neuron as a passive capacitor connected by a linear leaky resistor. Using LIF model in a 3D system will change the key features of neurons membrane. Therefore, neuronal membrane voltage will be changed accordingly. From the TSV property serving as membrane capacitor in this work, we modified the LIF model and the circuit model of neuron membrane using TSV is shown in Figure 9.

Figure 9. Circuit Model of LIF neuron in 3D IC

The membrane capacitance model basically describes the electrical activity of neuron corresponding to the ionic charge diffusion through the membrane. The current flow through the leak channels of the neurons membrane is given by,

$$I_c = G_L(V_m - E) \quad (1)$$

where G_L is the leaky conductance, V_m is the membrane potential, and E is the equilibrium potential.

Change in membrane potential due to the current flow depends on membrane capacitance as the charges accumulate. The rate of change of the total charge in a membrane capacitance gives the current through it as,

$$I_c(t) = -\frac{\partial Q(t)}{\partial t} \quad (2)$$

Therefore, the RC behavior of the membrane model is expressed as below,

$$C_m \frac{\partial V_m}{\partial t} = -G_L(V_m - E) + I_0 \quad (3)$$

where C_m is the membrane capacitance, and I_0 is the applied steady current.

For the TSV as membrane capacitance C_m , the space charge and surface potential of the MIS structure of TSV determine its capacitance-voltage characteristics. The total charge on the TSV can be calculated by integrating the electric field through the surface as,

$$Q_m = -2\pi \times r_{ox} \times L \times \epsilon_{Si} \times \frac{\partial \phi}{\partial r} \Big|_{r=r_{ox}} \quad (4)$$

where, r_{ox} is the TSV oxide outer radius, L is the length of TSV, ϵ_{Si} is permittivity of silicon, and ϕ is the charge potential.

Now, the TSV capacitance which will serve as membrane capacitance can be obtained from the total charge and TSV potential as below,

$$C_m = \frac{Q_m}{V_m} \quad (5)$$

where, V_m is the TSV surface potential.

The total TSV capacitance is parallel to the leakage resistor as demonstrated in Figure 9.

While the typical membrane capacitance values of 0.5 – 1 pF corresponds to 50 – 200 μm^2 capacitors [5], a signal TSV with multiple ground TSVs (up to 8) estimates 90 – 130 fF of capacitance [20]. Therefore, it is necessary to increase the TSV capacitance to meet the requirement of membrane capacitance in 3D neuromorphic IC.

4. BUMP OXIDE CAPACITANCE MODEL

To conduct an excellent reliability test, the importance of interconnection mechanism of TSV based 3D IC using solder bumps (Figure 10) has already been proven [21]. The physical dimension of the bump is significantly larger compared to the dimension of TSV as demonstrated in [22]. Hence, adding an additional layer of oxide around the bump increases its capacitance appreciably and consequently increases the overall TSV capacitance.

A new TSV structure is proposed in 3D chips as demonstrated in Figure 11. In this structure, the isolation silicon dioxide outside the bump contact area is introduced, which will contribute an additional parasitic capacitance due to the higher dielectric constant of SiO_2 compared to the small air gap surrounding the bump. This capacitance will be formed between the lateral side of the bump and the conductive silicon substrate which would be accounted to calculate the total TSV parasitic capacitances [23 - 24].

When, TSV is buried in Si substrate, the TSV capacitance will be the capacitance of two wire transmission line with dielectric loss layer. It is given by the equation below,

$$C_{TSV} = \frac{\pi \epsilon_0 \epsilon_{Si} [1 - j(\tan \delta_d + 1/\omega \epsilon_0 \epsilon_{Si} \rho_{Si})]}{\ln \left[\left(\frac{d_{TSV}}{2r_{ox}} \right) + \sqrt{\left(\frac{d_{TSV}}{2r_{ox}} \right)^2 - 1} \right]} \quad (6)$$

where, d_{TSV} is the pitch between the TSV, ϵ_0 is the permittivity of vacuum, ρ_{Si} is the resistivity of substrate material, and $\tan \delta_d$ is the polarization loss of Si.

The per unit length capacitance for oxide layer of conventional TSV structure can be found by using the formula of coaxial capacitance. The cylindrical capacitance with the TSV conductor radius of r_{TSV} and oxide outer radius of r_{ox} is given by,

$$C_{ox} = \frac{\pi \epsilon_0 \epsilon_{ox}}{\ln \left(\frac{r_{ox}}{r_{TSV}} \right)} \quad (7)$$

where, ϵ_{ox} is the permittivity of the dielectric silicon-di-oxide.

Figure 10. TSV bump (a) In 3D IC [21] (b) Cross-sectional SEM image [22]

Once, oxide is introduced to the lateral side of bump, the coaxial capacitance is formed and it is expressed by the following equation,

$$C_{Bump_ox} = \frac{\pi \epsilon_0 \epsilon_{ox}}{\ln\left(\frac{r_{Bump} + t_{ox}}{r_{Bump}}\right)} \quad (8)$$

where, t_{ox} is the thickness of oxide at bump, and r_{Bump} is the radius of bump.

For the estimation of total capacitance of the proposed TSV structure, we need to sum up the capacitance of conventional two TSV with bump and the capacitance induced by introducing bump oxide. The proposed TSV capacitance will be,

$$C_{TSV_total} = \frac{(C_{ox} + C_{Bump_ox})C_{TSV}}{C_{ox} + C_{Bump_ox} + C_{TSV}} \quad (9)$$

Figure 11. Proposed TSV structure with oxides around the bumps

In our proposed methodology, silicon-di-oxide and air are the dielectric between the bump of the TSV. Hence we get the relationship below,

$$C_{Bump_proposed} = C_{Bump_ox} + C_{Bump_air} \quad (10)$$

Now, it can be found from the equation above that, our proposed method could significantly increase the bump capacitance as well as total TSV capacitance. Also, the TSV-Si substrate-TSV capacitance can be presented as parallel plate capacitance. Therefore, the total TSV capacitance will be enhanced which is required to store the internal membrane voltage.

By using the above mentioned method, the TSV capacitance could be enhanced significantly which will greatly improve the implementation of 3D neural system by serving as membrane capacitance. The simulation results are discussed in the next section.

5. RESULTS AND ANALYSIS

To evaluate the effectiveness of the proposed structure and method, the capacitance, the voltage, and the current in a 3D NM IC are simulated and compared to the ones using the conventional method. To conduct the simulation, a simple LIF neuron model is employed.

5.1 Capacitance Enhancement

The capacitance of TSVs including one pair of signal and ground using oxide around the bump are plotted in Tables 2-3 for wafer level, and chip level respectively. The simulated capacitances using the conventional and the proposed TSV structures show significant differences for both the bonding types of TSVs. It can be seen that more than 15% capacitance is increased through the addition of bump oxide.

Table 2. TSV capacitance using conventional and proposed method (wafer level TSV)

Freq (MHz)	10	20	30	40	50
Conventional Cap (fF)	204	203	201	199	197
Proposed Model (fF)	250	248.8	246	242.4	238
% Improved	22.5	22.4	22.3	21.8	20.8
Freq (MHz)	60	70	80	90	100
Conventional Cap (fF)	194.6	191.2	188	184	180
Proposed Model (fF)	234	229	222.4	216	208
% Improved	20.2	19.7	18.3	17.4	15.6

Table 3. TSV capacitance using conventional and proposed method (chip level TSV)

Freq (MHz)	10	20	30	40	50
Conventional Cap (fF)	624	622	618	614	610
Proposed Model (fF)	766	760	754	748	740
% Improved	22.7	22.1	22.0	21.8	21.8
Freq (MHz)	60	70	80	90	100
Conventional Cap (fF)	604	596	586	574	560
Proposed Model (fF)	730	718	704	684	664
% Improved	20.8	20.4	20.1	19.2	18.6

For wafer level TSV, the capacitance is improved from 15.6% - 22.5% and for chip level TSV, it is improved from 18.6% - 22.7%. This is a significant improvement of capacitance using a pair of signal and ground TSV. Besides, the frequency dependent simulation result shows that, the TSV capacitance is decreasing while frequency is increasing. This is because of the electrical field becoming less confined in SiO_2 layer and penetrates in Si region.

5.2 Membrane Spike Response

To demonstrate the effectiveness of a neuron, the membrane capacitance implemented by employing TSVs, a 3D model of neuron is constructed and its performance is simulated in SPICE. The simulation results are compared to the ones using LIF model. The comparisons are illustrated in Figure 12 to Figure 13. It is clear that the voltage and current of the TSV based 3D neuron proposed in this work are comparable to the LIF model based neuron. It is observed that the spike frequency for both the voltage and current is also increased when the TSV based neuron is used, and which could ensure a higher volume of information. The threshold

potentials are the same for both models despite the different in spike length and reset voltage which may potentially result from the difference in their capacitance values. A similar behavior is also observed for the neuronal current in both models.

Figure 12. Spike response (voltage) of 3D model and LIF model of neuron

Figure 13. Spike response (Current) of 3D model and LIF model of neuron

Due to the enhanced capacitance in the proposed design, it can achieve long time constant and this is necessary for communicating with the external world in real time.

6. CONCLUSION

With the trend of energy efficiency in modern system, TSV based 3D neuromorphic chip could exhibit higher performance which are very competitive for the next generation potential technology in neuromorphic hardware system. In this work, we investigated the TSV properties that can be used as membrane capacitance and significantly benefits the system. Also, a new technique has been proposed that could significantly enhance the TSV capacitance in 3D neuromorphic system. This increasing capacitance is necessary to deal with the neuronal membrane potential which performs the key activity in 3D neural systems.

7. REFERENCES

- [1] P. Camilleri, M. Giulioni, V. Dante, D. Badoni, G. Indiveri, B. Michaelis, et al., "A neuromorphic aVLSI network chip with configurable plastic synapses," in *Proc. Int. Conf. HIS*, Sep. 2007, pp. 296–301.
- [2] T. J. Koickal, A. Hamilton, S. L. Tan, J. A. Covington, J. W. Gardner, T. C. Pearce, "Analog VLSI Circuit Implementation of an Adaptive Neuromorphic Olfaction Chip," *IEEE Trans. Circuits Syst.* 54, 1(Jan. 2007), 60–73.
- [3] Y. Yi, P. Li, V. Sarin, and W. Shi, "Impedance extraction for 3-D structures with multiple dielectrics using preconditioned boundary element method," in *proc. IEEE/ACM Int. Conf. Computer-Aided Design*, 2007, pp. 7–10.
- [4] Y. Yi and Y. Zhou, "A novel circuit model for multiple Through Silicon Vias (TSVs) in 3D IC," in *proc IEEE Int. 3D Systems Integration Conf. (3DIC)*, 2013, pp. 1–4.
- [5] A. Joubert, M. Duranton, B. Belhadj, O. Temam, and R. Heliot, "Capacitance of TSVs in 3D stacked chips a problem? Not for neuromorphic systems," in *Proc. DAC'12*, 2012, pp. 1260–1261.
- [6] B. Belhadj et al., "The improbable but highly appropriate marriage of 3D stacking and neuromorphic accelerators," in *Proc. CASES'14*, pp. 1–9.
- [7] G. Indiveri, and S. C. Liu, "Memory and Information Processing in Neuromorphic Systems," in *Proc. of the IEEE*, vol. 103, no. 8, pp. 1379–1397, Aug. 2015.
- [8] F. Akopyan et al., "TrueNorth: Design and Tool Flow of a 65 mW 1 Million Neuron Programmable Neurosynaptic Chip," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Syst.*, vol. 34, no. 10, pp. 1537–1557, Oct. 2015.
- [9] J. M. Cruz-Albrecht, M. W. Yung, and N. Srinivasa, "Energy-efficient neuron, synapse and STDP integrated circuits," *IEEE trans. biomedical circuits and systems*, vol. 6, no. 3, pp. 246–256, 2012.
- [10] R. Wang, C. S. Thakur, T. J. Hamilton, J. Tapson, and A. van Schaik, "A compact aVLSI conductance-based silicon neuron," pp. 1–4.
- [11] J. H. Wijekoon, and P. Dudek, "Compact silicon neuron circuit with spiking and bursting behaviour," *Neural Networks*, vol. 21, no. 2, pp. 524–534, 2008.
- [12] C. Zhao, B. T. Wysocki, Y. Liu, C. D. Thiem, N. R. McDonald, and Y. Yi, "Spike-time-dependent encoding for neuromorphic processors," *ACM Journal Emerging Tech. Comp. Syst.*, vol. 12, no. 3, pp. 23, 2015.
- [13] J. M. Cruz-Albrecht, M. W. Yung, and N. Srinivasa, "Energy-efficient neuron, synapse and STDP integrated circuits," *IEEE trans. biomedical circuits and systems*, 6(3):246–256, 2012.
- [14] C. Hwang, B. Achkir, and J. Fan, "Capacitance-Enhanced Through-Silicon Via for Power Distribution Networks in 3D ICs," in *IEEE Electron Device Letters*, 37,(4):478–481, April 2016.
- [15] D. Fick et al., "Centip3De: A Cluster-Based NTC Architecture With 64 ARM Cortex-M3 Cores in 3D Stacked 130 nm CMOS," *IEEE Journal of Solid-State Circuits*, 48,(1), pp.104–117, 2013
- [16] J. H. Lau, "TSV Manufacturing Yield and Hidden Costs for 3D IC Integration," in *Proc. Of Electronic Components and Technology Conference (ECTC)*, pp. 1031–1042, 2010.
- [17] Y. Zhao, S. Khursheed and B. M. Al-Hashimi, "Cost-Effective TSV Grouping for Yield Improvement of 3D-ICs," in *Proc. Asian Test Symp.*, 2011, pp. 201–206.
- [18] C.-T. Ko, and K.-N. Chen, "Reliability of key technologies in 3D integration," *Microelect. Reliability*, vol. 53, no. 1, pp. 7–16, 2013
- [19] <http://electroiq.com/blog/2010/08/process-equipment/>
- [20] R. Weerasekera et al., "An Analytical Capacitance Model for Through-Silicon Vias in Floating Silicon Substrate," *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1182–1188, March 2016.
- [21] K. W. Paik, Y. Choi and J. Shin, "3D-TSV vertical interconnection method using Cu/SnAg double bumps," in *Proc. IEEE Int. Workshop Low Temp. Bonding 3D Integr.*, 2012, pp. 215–215.
- [22] D. H. Jung et al., "Frequency and time domain measurement of through-silicon via (TSV) failure," in *Proc. IEEE Conf. Elect. Perform. Electronic Packag. Syst.*, 2012, pp. 331–334.
- [23] M. A. Ehsan, Z. Zhou, L. Liu and Y. Yi, "An Analytical Through Silicon Via (TSV) Surface Roughness Model Applied to a Millimeter Wave 3-D IC," *IEEE Trans. Electromag. Compat.*, vol. 57, no. 4, pp. 815–826, Aug. 2015.
- [24] Y. Yi and Y. Zhou, "A novel circuit model for multiple Through Silicon Vias (TSVs) in 3D IC," in *Proc. IEEE Int. 3D Systems Integr. Conf.*, 2013, pp. 1–4.