Design and Analysis of STTRAM-Based Ternary Content Addressable Memory Cell

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Content Addressable Memory (CAM) is widely used in applications where searching a specific pattern of data is a major operation. Conventional CAMs suffer from area, power, and speed limitations. We propose Spin-Torque Transfer RAM-based Ternary CAM (TCAM) cells. The proposed NOR-type TCAM cell has a 62.5% (33%) reduction in number of transistor compared to conventional CMOS TCAMs (spintronic TCAMs). We analyzed the sense margin of the proposed TCAM with respect to 16-, 32-, 64-, 128-, and 256-bit word sizes in 22nm predictive technology. Simulations indicated a reliable sense margin of 50mV even at 0.7V supply voltage for 256-bits word. We also explored a selective threshold voltage modulation of transistors to improve the sense margin and tolerate process and voltage variations. The worst-case search latency and sense margin of 256-bit TCAM is found to be 263ps and 220mV, respectively, at 1V supply voltage. The average search power consumed is 13mW, and the search energy is 4.7fJ/bit search. The write time is 4ns, and the write energy is 0.69pJ/bit. We leverage the NOR-type TCAM design to realize a 9T-2 Magnetic Tunnel Junctions NAND-type TCAM cell that has 43.75% less number of transistors than the conventional CMOS TCAM cell. A NAND-type cell can support up to 64-bit words with a maximum sense margin of up to 33mV. We compare the performance metrics of NOR- and NAND-type TCAM cells with other TCAMs in the literature.

CCS Concepts: • **Hardware** → **Integrated circuits**; **Non-volatile memory**; **Spintronics and magnetic technologies**

Additional Key Words and Phrases: Magnetic Tunnel Junction, nano-CAM, NOR topology TCAM, NAND topology TCAM

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1. INTRODUCTION

Content Addressable Memory (CAM) finds numerous applications in pattern matching, Internet data processing, packet forwarding, and storage of tag bits in processor cache and as associative memory. The special functionality of the content search in CAM requires a comparison circuitry integrated with the memory cell [Pagiamtiz et al. 2006]. The comparator in addition to a memory element adds area and power overhead

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Fig. 1. (a) 4-T 2-MTJ TCAM [Matsunaga et al. 2012]; (b) schematic of DWM cells; (c) DWM CAM realization [Zhang et al. 2012].

in CAMs. The need to store and match “don’t care” requires two storage bits, which further worsens the area overhead. CMOS CAM is power hungry due to power consumed in Match Line (ML), search line, and leakage of the bit cell. In nanometer technologies, leakage power constitutes a major fraction of the total power consumed in CAM memory [Karam et al. 2015]. Non-volatile technologies that are more area efficient than a SRAM and also can provide zero leakage are attractive in such a scenario [Pagiamtiz et al. 2006; Shen et al. 2006]. Area efficiency and non-volatility of Spin-Torque Transfer RAM– (STTRAM) based ternary CAM is very useful for on-chip CAM applications. Numerous works have demonstrated the realization of CAM using non-volatile memory technologies like memristor [Junsangsri et al. 2012], Resistive RAM (ReRAM) [Li et al. 2014], and spintronic elements such as Domain Wall Memory (DWM), Magnetic Tunnel Junctions (MTJ), and STTRAM [Xu et al. 2008; Nebashi et al. 2011; Zhang et al. 2012; Chen et al. 2013]. Memristor-based NOR Ternary Content Addressable Memory (TCAM) [Junsangsri et al. 2012] uses a voltage divider network formed by the memristors to enable the discharging path to discharge the match line depending on match/miss. It incurs higher write delay of up to 800ns, which hurts the table update performance in the network routers application. ReRAM-based TCAM [Li et al. 2014] employs a special clocked self-referenced sensing scheme that complicates the memory system design due to additional reference ML required. An efficient integration of a spintronic device with CMOS technology has motivated us to employ them in TCAM cell design. Also, the principle of bit storage and writing methodologies differ in memristor and ReRAM compared to spintronic devices such as MTJ and DWM. This limits the direct extension of memristive and ReRAM TCAMs to design spintronic TCAMs.

Spintronic CAMs using MTJ and DWM (Figure 1) suffer from issues such as larger area, unreliable write operation, high search delay, and high power consumption

Fig. 2. (a) Conventional NOR-type TCAM and (b) conventional NAND-type TCAM. Bit-drieline access transistors are not shown in the figure for simplicity.

compared to CMOS CAMs [Karam et al. 2015]. The MTJ-based TCAM 4T-2MTJ design (Figure 1(a)) [Matsunaga et al. 2012] is area and power efficient; however, it employs a technique-based proportional total current drawn from the ML by bit cells in words. Further, the circuit uses both NMOS and PMOS transistors. In this technique, the sense margin decreases significantly as the number of bits increases in the worst-case search of a single bit miss. So the design is not scalable beyond a certain word length (144 bits). Figure 1(b) shows DWM cells in the memory architecture that consists of read heads along a nanowire storing data bits. The DWM-based TCAM shown in Figure 1(c) uses 12 transistors. Therefore, deployment of non-volatile memory in CAM requires effort to achieve a smaller footprint and better performance in terms of search delay, write delay, write power, and search power. A NOR-type MTJ-based TCAM is proposed [Govindaraj et al. 2015] that can support wider CAM words while being tolerant to voltage and temperature variations. However, it is susceptible to a poor sense margin due to process variations. We propose Search Enable (SE) modulation to improve the sense margin under inter-die process variation. We also propose multi- V_{TH} design to improve the sense margin. We also propose a NAND-type TCAM that exploits the NOR TCAM design. The proposed NOR-type TCAM employs only 6 transistors and 2 MTJs instead of 16 transistors in a CMOS TCAM, and a NAND TCAM cell uses 9 transistors and 2 MTJs compared to a NAND CMOS TCAM, which uses 16 transistors. In the following paragraphs, we provide an overview of the CAM and STTRAM technologies.

1.1. Content Addressable Memory

CAMs can be divided into two categories depending on the number of states that can be stored in the memory cell, namely Binary CAM (BCAM) and TCAM. BCAM stores a binary bit, that is, “0” and “1,” whereas TCAM can store three possible values, namely “don’t care” (X), “1,” and “0.” CAMs can be further categorized into two topologies, namely NOR and NAND (Figures 2(a) and (b)). The stored bits are compared with the data on the Search Line (SL) and its complement ($\overline{SL}$) by an XOR operation with the transistor network M1, M2, M3, and M4. To store data in a TCAM cell of a NOR-type architecture, the data bit and the complement are stored in two SRAM cells. The *don’t care* bit can be realized by storing “1” in both SRAM cells, that is, $D = \overline{D} = 1$. In case of a match, both the $SL-D$ and $\overline{SL}-\overline{D}$ paths are disconnected, and the match line remains precharged. In case of a miss, either of the $SL-D$ or $\overline{SL}-\overline{D}$ connect ML to ground, which discharges the precharged ML. In a NAND-type architecture, TCAM cells are connected in series (Figure 1(b)). Data bit D and $\overline{D}$ are derived from a single SRAM cell, unlike two SRAM cells in a NOR-type TCAM. The stored bit is masked by using a mask bit (M) in a parallel SRAM cell. In the case of a match, the precharged

Fig. 3. (a) MTJ in anti-parallel (“1”) and parallel (“0”) states and (b) the directions of charge current to write “1” and “0.”

Table I. MTJ Parameters Used

Parameter	Value
Saturation Magnetization (Ms)	800Oe
Critical current density (I_{co})	3.2 MA/cm^2
Uniaxial Anisotropy (Ku)	150150 erg/cc
Damping Constant	0.007
TMR	125%
Length and Width	$60\text{nm} \times 60\text{nm}$
Critical Current (I_{co})	$115\mu\text{A}$

ML is connected to ground by series TCAM cells of the word by turning the NMOS transistor M1 ON. Storing the mask bit as “1” enables transistor M2 despite match or miss, which implements the *don’t care* functionality. CMOS TCAM uses two SRAM cells, which doubles the area overhead compared to conventional SRAM cell.

1.2. STTRAM

STTRAM is a spintronic-based memory cell that stores the data in the form of the spin of an electron, unlike a static CMOS memory cell, which stores data in the form of electric potential. The basic storage element is a MTJ that consists of three layers, a layer of magnetic oxide sandwiched between the other two layers of magnetic materials. Data are stored in the form of magnetization in the two magnetic layers. Bit “0” (“1”) is stored when the two magnetic layers are magnetized in the same (opposite) direction. Figure 3(a) shows an MTJ device configuration in the parallel and antiparallel states. A Pinned Layer (PL) has fixed magnetization while Free Layer (FL) magnetization can be polarized parallel or anti-parallel with respect to the PL. The resistance of MTJ is high when PL and FL are in antiparallel configuration whereas the resistance is low when they are parallel to each other. The value written to the STTRAM bit depends on the direction and the strength of the charge current. Minimum current required to flip the state of the MTJ in a STTRAM bit is called critical current. Figure 3(b) shows the direction of current to write “1” and “0” to MTJ [Fong et al. 2013]. Tunnel Magneto Resistance (TMR) is the ratio that determines the ratio of electrical resistances of the MTJ structure in parallel and antiparallel polarization states of FL relative to PL magnetization. If R_H (R_L) is the MTJ resistances in antiparallel (parallel) states, then the TMR is defined as $TMR = \frac{R_H - R_L}{R_L}$. In this article, MTJ and the transistors in series together is referred to as STTRAM, while MTJ refers to the MTJ device in the memory cell. Table I summarizes the parameters of the MTJ device used in this work.

The rest of the article is organized as follows. Section 2 discusses the proposed TCAM cells design concept and circuit operation. The design analysis of a NOR-type TCAM is

Fig. 4. Proposed TCAM cell.

presented in Section 3, and simulation results are discussed in Section 4. Simulations results of NAND-type TCAM are discussed in Section 5, and the comparative analysis is presented in Section 6. Conclusions are drawn in Section 7.

2. PROPOSED TCAM CELLS

In this section, first we discuss the structure of the proposed TCAM. Next, we present qualitative analysis and describe read, write, and search operations.

2.1. NOR TCAM Cell Circuit

The circuit diagram of the proposed TCAM is shown in Figure 4. Two MTJs store D and $\bar{D}$, respectively. Transistors M1 and M2 form an ML discharge network depending on the result of data comparison with the search lines SL and $\bar{SL}$. During a search, transistors M3/M5 and M4/M5 along with the MTJ resistance due to TMR make a voltage divider network in which the drain voltages of M3/M4 drive the gates of discharge transistors M1/M2. The cell is designed in such a way that during *match* the voltage of nodes X1 and X2 is below the threshold voltage of M1 and M2, and the ML stays precharged. However, during a *mismatch*, the voltage of X1 and X2 rises above the threshold voltage of M1 and M2, respectively, discharging the ML.

Transistor M3/M4 are the wordline (WL) selection transistors, and M6 is the write access transistor that turns ON only during write (WR) operation. Transistor M6 is sized larger to allow sufficient write current. Transistor M5 is driven by an SE signal and, sized to limit the current through STTRAM bit for read disturb free search operation. The don't care bit can be stored in the cell by storing "1" in both the D and $\bar{D}$ bits. The search bit can be masked by driving $SL = \bar{SL} = 0$ on the search lines. The Source Line (SrL) is used for two purposes, namely (a) a write operation when the SrL is connected to 0 or V_{dd} depending on the write data to the MTJs and (b) a search operation when SrL is driven to 0 to allow voltage division.

2.2. Qualitative Analysis of the Cell Design

There are two match cases, namely (a) $(D, \bar{D}) = (SL, \bar{SL}) = (1, 0)$ and (b) $(D, \bar{D}) = (SL, \bar{SL}) = (0, 1)$. Since both cases are identical, we will only explain the first case. For $(D, \bar{D}) = (1, 0)$, the left-side MTJ is in a high resistance (R_H) state, whereas the right side MTJ is in a low resistance (R_L) state. Since $(SL, \bar{SL}) = (1, 0)$, the voltage at node X1 is $V_{X1} = V_{SL} * \frac{r}{R_H + r} = V_M$ and the voltage at node X2 is a voltage drop due to current flow from node X1 to $\bar{SL}$ (detailed analysis is given in Section 2.4). In this expression, r is the lumped ON resistance of transistors M3, M4, and M5 (Figure 5) and V_{SL} is the SL voltage. To keep transistor M1 OFF during a match, V_{X1} should be lower than V_{TH0} (i.e., the threshold voltage of M1 and M2).

Fig. 5. Equivalent circuit during (a) write operation; the left-side STTRAM resistance is R_H ($D = "1"$) and the right-side STTRAM resistance is R_L ($\bar{D} = "0"$). (b) Search operation. Equivalent circuit while (c) match M1 and M2 are turned ON; and (d) mismatch M1 and M2 are OFF as $V_{d1} < V_{th0}$.

For the mismatch, there are two cases, namely (a) $(D, \bar{D}) = (1, 0)$ and $(SL, \bar{SL}) = (0, 1)$ and (b) $(D, \bar{D}) = (0, 1)$ and $(SL, \bar{SL}) = (1, 0)$. For the first case, the voltage at node X_1 is $V_{X1} = V_{\bar{SL}} * \frac{R_H}{R_H + r_{eff}} = V_{MM1}$, where r_{eff} is the effective resistance of R_L, r_3, r_5, r_4 is the resistive network. The voltage at X_2 is $V_{X2} = V_{\bar{SL}} * \frac{r}{R_L + r} = V_{MM2}$, where $V_{\bar{SL}}$ is the $\bar{SL}$ voltage. To keep transistors M1, M2 ON during mismatch, V_{MM1} , and V_{MM2} should be higher than V_{TH0} . Similar analysis applies to case (b).

From the above equations, $V_{MMX} > V_{MX}$ for the two cases as $R_H > R_L$. For the design to function properly (i.e., discharge ML during *mismatch* at a higher speed compared to that of a *match* case), R_H, R_L , and r should be selected such that $V_{MX} < V_{th0} < V_{MMX}$. The following analytical equations can be used to quantify the design parameters:

$$V_{MM} = V_{dd} - I_{MM} * R_L = V_{\bar{sl}} * \frac{r}{R_L + r} = V_{th0} + \Delta_1, \quad (1)$$

$$V_M = V_{dd} - I_M * R_H = V_{sl} * \frac{r}{R_H + r} = V_{th0} - \Delta_2, \quad (2)$$

where I_{MM} and I_M are the currents drawn from SL and $\bar{SL}$ in the cases of mismatch and match, respectively, and Δ_1, Δ_2 are the offset voltages with respect to V_{th0} .

Subtracting (1) and (2) and using $R_H = R_L * (1 + TMR)$, we obtain

$$V_{MM} - V_M = V_{dd} \left(\frac{r}{R_L + r} - \frac{r}{R_H + r} \right) = \Delta_1 + \Delta_2, \quad (3)$$

Fig. 6. V_{gs} margin diagram illustrating best and worst V_M and V_{MM} with respect to V_{th0} .

Table II. States of Control Signals NOR TCAM Memory Operations

	Write operation: $WR = V_{dd}$, $SE = 'X'$					
	Write D bit			Write $\bar{D}$ bit		
	$WL1 = V_{dd}$, $WL2 = 0$			$WL1 = 0$, $WL2 = V_{dd}$		
	SL	$\overline{SL}$	SrL	SL	$\overline{SL}$	SrL
Write “1”	0	X	V_{dd}	X	V_{dd}	0
Write “0”	V_{dd}	X	0	X	0	V_{dd}
Write “X”	0	0	V_{dd}	$WL1 = WL2 = V_{dd}$		
	Search operation: $WL1 = WL2 = V_{dd}$, $WR = 0$, $SE = V_{dd}$					
	SL		$\overline{SL}$		SrL	
Search “1”	V_{dd}		0		0	
Search “0”	0		V_{dd}		0	
Masking the Search	0		0		0	

$$V_{MM} - V_M = V_{dd} \left[\frac{r * R_L * TMR}{(R_L + r)(R_L(1 + TMR) + r)} \right] = \Delta_1 + \Delta_2. \quad (4)$$

The optimization of the proposed TCAM revolves around three key requirements: (a) maximizing the difference between the mismatch and match voltages, that is, $(\Delta_1 + \Delta_2)$; (b) maximizing the absolute values of offsets from V_{TH0} , that is, $|\Delta_1|$ and $|\Delta_2|$ to keep M1/M2 strongly ON or OFF as needed during mismatch and match, respectively; and (c) lowering the search current below critical write current of MTJ.

From Equation (4), it can be concluded that higher TMR, higher R_H , and higher r can be employed to enhance $(\Delta_1 + \Delta_2)$. Although higher r and R_L is also good for maximizing Δ_1 , it minimizes Δ_2 . A lower Δ_2 can turn ON M1/M2 during match degrading the sense margin. Figure 6 shows a pictorial representation of this situation with three operating points. The voltages V_{MM1} , V_{MM3} , V_{M1} , and V_{M3} provide a poor sense margin compared to V_{MM2} and V_{M2} even with same magnitude of $\Delta_1 + \Delta_2$. The ideal margin is obtained when $R_H = \infty$ and $R_L = 0$, which gives $V_{MM} = V_{dd}$ and $V_M = 0$. However, a lower R_L could be detrimental for read disturb due to high search current. High values of R_H and R_L ensure the low search line currents. This, in combination with high TMR, can provide a better V_{gs} margin, that is, $(\Delta_1 + \Delta_2)$, with low search power consumption. The design optimization conducted in this article accounts for the above factors.

2.3. Write Operation

In the proposed TCAM, the search lines SL and $\bar{SL}$ are used to write data to the STTMRAM bits. Table II summarizes the states of control signals in the write operation. Writing "1" and "0" consumes two cycles to write to the two STTMRAMs while "X" can

be written in a single cycle. During the write, the ML precharge is disabled to avoid power consumption from the ML. This is achieved by pulling the “precharge” signal high. NMOS transistor M6 is turned ON during write by the WR signal. Note that M6 is sized to provide the drain current greater than the critical write current of the STTTRAM. The state of search enable signal SE is “Don’t care” as M5 is connected parallel to M6. For the analysis, we assume that SE is pulled low. The WL is turned ON only for the selected word so the unselected cells are unaffected. The source line SrL is controlled appropriately to write a “1” or “0.” Figure 5(a) shows the equivalent circuit of TCAM cell during write. The transistors are replaced with equivalent ON resistances. Resistors r_3 , r_4 , and r_6 are equivalent resistors of M3, M4, and M6 respectively. The writing operation is described below. In the first cycle of the write operation, writing to the D bit is enabled by pulling WL1 to V_{dd} , and the $\bar{D}$ bit path is disabled by pulling WL2 to ground. In the second cycle of the write operation, writing to the $\bar{D}$ bit is enabled by pulling WL2 to V_{dd} , and the D bit path is disabled by pulling WL1 to ground. Direction of charge current through the MTJ is pictorially represented in Figure 3(b) to write parallel and anti-parallel states.

1. Writing “1”: In the first cycle, SrL is pulled high, and the SL line is pulled to ground. The write current flows from SL writing an antiparallel state to the STTTRAM storing bit D. There is no current through the other STTTRAM bit as the WL2 control signal is grounded. In the second cycle, the SrL is pulled low, $\bar{S}L$ is pulled to V_{dd} , and WL2 is pulled high, which programs the other STTTRAM storing $\bar{D}$ to the parallel state. There is no current through the other STTTRAM bit as WL1 is grounded.
2. Writing “0”: In the first cycle, the SL is pulled high and the SrL line is pulled low. This cycle writes parallel magnetization state to the STTTRAM storing the D bit. In the second cycle, the SrL is pulled high while $\bar{S}L$ is at 0, which programs the $\bar{D}$ bit to an antiparallel state.
3. Writing “X”: The “X” state can be stored by writing logic 1 to both D and $\bar{D}$. The SrL is pulled to V_{dd} , and the search lines SL and $\bar{S}L$ are pulled low. The current flows through both the STTTRAMs storing antiparallel states to D and $\bar{D}$.

2.4. Search Operation

Search is a single-cycle operation in CAM. The ML is precharged to V_{dd} , and WR is pulled to ground. The SrL is pulled to ground throughout the search operation. Next, SE and WL are pulled high to enable the conducting path through M5 and M3/M4 (Table II). Either V_{MM} or V_M voltage is developed depending on the match or mismatch, respectively, at the gate of M1/M2. The search lines SL is pulled to V_{dd} and $\bar{S}L$ is pulled low to search a bit “1.” Similarly, SL is pulled low and $\bar{S}L$ is pulled to V_{dd} to search for bit “0.” Both SL and $\bar{S}L$ are pulled low to search “X.” Circuit operation in match and mismatch cases are discussed below. Figure 5(b) shows the equivalent circuit during search operation.

1. Match: Let $(D, \bar{D}) = (SL, \bar{S}L) = (1, 0)$. Voltages V_{X1} and V_{X2} at the nodes X_1 and X_2 (Figure 4) are given by

$$V_{X1} = V_{dh} = V_{dd} * \frac{r_3 + (r_5 || (r_4 + R_L))}{R_H + r_3 + (r_5 || (r_4 + R_L))}$$

$$V_{X2} = V_{dl} = V_{dd} * \frac{(r_5 || (r_4 + R_L)) * R_L}{(R_H + r_3 + (r_5 || (r_4 + R_L)))(r_4 + R_L)}$$

Fig. 7. Waveform showing the search operation. Match line voltages during the mismatch and match cases for 1-, 16-, 128-, and 256-bit word sizes are shown.

Note that V_{X2} is less than V_{X1} and appears due to the potential across $r5$, which results in a current though R_L even when $\bar{S}L = 0$ (Figure 5(c)). The transistors M3 and M5 are sized such that $V_{X1} < V_{th0}$. So M1/M2 are turned OFF and the ML remains precharged. The other match case, that is, $(D, \bar{D}) = (SL, \bar{S}L) = (0, 1)$, is similar.

2. Mismatch: Let $(D, \bar{D}) = (1, 0)$ and $(SL, \bar{S}L) = (0, 1)$. Then,

$$V_{X1} = V_{dl} = V_{dd} * \frac{r4 + (r5 || (r3 + RH))}{R_L + r4 + (r5 || (r3 + RH))}$$

$$V_{X2} = V_{dh} = V_{dd} * \frac{(r5 || (r4 + R_H)) * R_H}{(R_H + r4)(R_L + r3 + (r5 || (r4 + R_H)))}$$

$V_{dl}(\text{miss}) > V_{th0} > V_{dh}(\text{match})$. Under these conditions (Figure 5(d)) both M1 and M2 are turned ON to discharge the precharged ML which provides better sense margin. Figure 7 illustrates the ML voltages during search operation for TCAM of varied word sizes namely 1-, 16-, 128-, and 256-bit for match and mismatch. Predictive 22nm model is used for simulations [Cao et al. 2002]. The waveforms correspond to the worst-case sense margin, that is, single miss in the whole word. The rate of discharge of ML line in match case increases with the word size due to the more number of cells leaking the ML current through weakly driven M1/M2. This in turn limits the sense margin for larger word sizes. The equations V_{X1} and V_{X2} can be also be derived for the transistor device parameters by replacing the voltage across transistor by V_{ds} and drain current of the transistors by the current through MTJ as below. The objective is to optimize the sense margin and search power and limit the drain current below the critical current of the MTJ. I_{d3} , I_{d4} , I_{d5} , are drain currents and V_{ds3} , V_{ds4} , V_{ds5} , are the drain to source voltages of transistors M₃, M₄, M₅, respectively. I_{c0} is the STTRAM critical current.

1. Match: Let $(D, \bar{D}) = (SL, \bar{S}L) = (1, 0)$. Voltages V_{X1} and V_{X2} at the nodes X_1 and X_2 (Figure 4) are given by

$$V_{X1} = V_{dh} = V_{dd} - (I_{d3} * R_H)$$

$$V_{X2} = V_{dl} = I_{d4} * R_L$$

$$I_{d3} = I_{d4} + I_{d5}; V_{ds5} = V_{ds4} + I_{d4} * R_L; I_{d4} \ll I_{c0} \text{ of the MTJs;}$$

$$V_{X1} > V_{X2} \ll V_{TH1}, V_{TH2}$$

Fig. 8. Proposed NAND configuration TCAM cell (Bit 0 stored).

2. Mismatch: Let $(D, \bar{D}) = (1, 0)$ and $(SL, \bar{SL}) = (0, 1)$. Then

$$V_{X1} = V_{dh} = V_{dd} - (I_{d4} * R_L)$$

$$V_{X2} = V_{dl} = I_{d3} * R_H$$

$$I_{d4} = I_{d3} + I_{d5}; V_{ds5} = V_{ds3} + I_{d3} * R_L; I_{d3} \ll I_{c0} \text{ of the MTJs};$$

$$V_{X1} > V_{X2} \gg V_{TH1}, V_{TH2}.$$

Drain currents and V_{ds} of transistors M_3, M_4, M_5 differ in case 1 and case 2. However, deriving analytical expressions for transistor parameters from the above expressions is straightforward but tedious with short channel transistor equations. We have adopted a simulation-based approach to minimize such efforts.

2.5. NAND-type TCAM Cell

Two types of TCAM topology are traditionally investigated in the literature, that is, NAND and NOR. Typically, NAND topology TCAM is faster compared to NOR topology TCAM in full CMOS realization. We investigate NOR and NAND topology TCAM realization using STTMRAM, which completes the study of STTMRAM-based TCAM design. In this section, we propose a NAND-type TCAM cell using STTMRAM.

Figure 8 shows the circuit diagram of a NAND-type TCAM cell along with the match line structure. The cell consists of 2 PMOS, 7 NMOS transistors, and 2 MTJs. We use the complementary method, that is, bit “1” is encoded by parallel magnetic spins and bit “0” is encoded as antiparallel states of relative magnetic spins, to realize NAND-type TCAM in this work. Six NMOS transistors M_1 – M_6 are sized for reliable search and write operation same as NOR-type TCAM explained earlier. In other words, the design analysis of NOR TCAM cell embedded in the NAND-type TCAM cell remain similar to that of a NOR-type cell. For a successful search operation in NAND TCAM, data bit “1” is encoded as a parallel state and bit “0” as an antiparallel state of the MTJ, respectively (Figure 8). Three additional transistors (M_7, M_8, M_9) are added on the basic NOR TCAM cell to realize the NAND-type TCAM cell. These additional transistors are of minimum size. For search operation, initially the match line is precharged, and the chain of PMOS transistors (M_9 in Figure 14) of individual TCAM cells connects the match line to V_{dd} only in the case of a complete match. Gates of PMOS transistors in the chain are precharged initially such that the chain is completely disconnected from V_{dd} . The search data and search enable signals are asserted after precharging of the match line. In the case of a match, the respective gate voltage is pulled low by the NMOS transistors M_1/M_2 in the search circuit. Thus, the match line is pulled high

Table III. States of Control Signals NAND TCAM Memory Operations

	Write operation: WR = V_{dd} , SE = 'X'					
	Write D bit WL1 = V_{dd} , WL2 = 0			Write $\bar{D}$ bit WL1 = 0, WL2 = V_{dd}		
	SL	$\overline{SL}$	SrL	SL	$\overline{SL}$	SrL
Write "1"	V_{dd}	X	0	X	0	V_{dd}
Write "0"	0	X	V_{dd}	X	V_{dd}	0
Write "X"	V_{dd}	V_{dd}	0	WL1 = WL2 = V_{dd}		
Search operation: WL1 = WL2 = V_{dd} , WR = 0, SE = V_{dd}						
	SL		$\overline{SL}$		SrL	
Search "1"	V_{dd}		0		0	
Search "0"	0		V_{dd}		0	
Masking the search	0		0		0	

to complete V_{dd} in the case of a complete match of a word. Table III summarizes the control signals in write and search operation of NAND TCAM. Writing is performed by injecting current more than the critical current from the search lines and source line (SrL). SE signal is "X," and Wr is pulled high throughout the write operation. Transistor M6 is sized to carry the current higher than the critical current of the MTJs for programmability. WL1 and WL2 are pulled to V_{dd} to enable writing the "D" bit and " $\bar{D}$ " bit, respectively, in the first and second cycles of write, respectively.

Write - 1: Bit "1" can be stored in two cycles of write, that is, by writing parallel state to the MTJ storing D-bit and anti-parallel state to the MTJ storing $\bar{D}$ bit. In the first cycle, WL1 and SL are driven to V_{dd} and SrL, and WL2 are pulled low, which results in current flow from a free layer to a fixed layer writing parallel state to the MTJ storing the "D" bit. In the second cycle, WL2 and SrL are precharged to V_{dd} , while WL1 and $\bar{S}L$ are pulled low. This results in the current flow from the PL to FL storing antiparallel state in the " $\bar{D}$ " bit.

Write - 0: Bit "0" is stored by writing an antiparallel state in the "D" bit and parallel state in " $\bar{D}$ " bit. In the first cycle, SrL and WL1 are precharged to V_{dd} , while SL is pulled to ground to write an antiparallel state to "D." In the second cycle, WL2 and $\bar{S}L$ are pulled to V_{dd} , while SrL is pulled low in order to write a parallel state to the " $\bar{D}$."

Write - X: The don't care bit is written by storing a parallel state in both the MTJs "D" and " $\bar{D}$," which results in a match case for both search bits "0" and "1." Writing "X" can be performed in a single cycle by pulling WL1, WL2, and SrL to V_{dd} and SL, and $\bar{S}L$ are pulled low to ground, which results in writing "0" (parallel state) simultaneously to both the MTJs.

Design analysis of NOR-type cell design is presented in the next section. We analyse the design parameter selections (MTJ resistance, TMR, and search transistors sizing) for successful search operation in TCAM. Design analysis for write operation remains the same as in a conventional STTRAM cell, which we have excluded in our work.

3. NOR TCAM CELL DESIGN ANALYSIS

In this section, first we present the methodologies to determine the sizing and MTJ resistance for reliable operation of the proposed NOR TCAM. We consider a broad range of word sizes in the analysis. In the proposed design, the parameters are optimized for sense margin and search power. Parameters for write current transistor M6 is chosen to drive sufficient write current. All the other parameters in the cell design are optimized for search operation.

Fig. 9. (a) Width of M5 v/s sense margin and STTRAM current from SL for various R_L (TMR = 100%). (b) Width of M3/M4 v/s sense margin and search current for various R_L .

3.1. Selection of R_L and NMOS Device

The low MTJ resistance and sizing of transistor M5 are chosen to keep the search current below the critical current while providing a sufficient V_{gs} to drive M1/M2 to differentiate the miss and match cases. Other than keeping the search current below critical current, limiting the search current is crucial to keep the search power as low as possible while achieving reliable sense margin. Moreover, ensuring the highest search current (through the lowest resistance) yields reliable design parameters, that is, total search current in the TCAM cell is less than the critical current under all PV (Process Variation) conditions. The high MTJ resistance is determined by the TMR. The transistor M6 is sized to provide write current greater than critical current through the STTRAM during write operation. We simulated a range of R_L (5k to 9k) with fixed TMR of 100%. The trend is shown in Figure 9(a) for a 16-bit word. It can be observed from the plot that high resistance values with smaller NMOS widths provide

Fig. 10. ML sense margin and search current from search line with respect to the width of NMOS M5 for different TMR values.

good sense margin (close to $V_{dd}/2$) with lower STTMRAM current from the search line. Based on this, $R_L = 8k\Omega$ is selected for the proposed design. The STTMRAM current during mismatch is also plotted. Note that mismatch current is always greater than the match current, and therefore we consider it for estimating the worst-case read disturb during search operation.

The widths of the NMOS devices M3/M4 and M5 are important parameters to ensure low search current and reduce the power dissipated from the search lines. Figure 9(a) shows the distribution of STTMRAM current for various widths of the NMOS device M5 with different R_L values. Smaller widths of NMOS offer high resistance, reduce search current (good for lower read disturb and power), and improve the sense margin (following the discussion in Section 2.2). However, minimum-sized transistor can be susceptible to manufacturing process variations. We selected 50nm for M5 width for the low search current. Further, two transistors of 100nm width in series can be used to minimize the process tolerance. It can be observed from the plot that miss case current is highly dependent on the width of the M5 NMOS device and remains almost same for different R_L values. High R_L is selected to keep the TMR within practical limits (100–150%) [Chun et al. 2013]. To determine the optimal size of transistors M3/M4, we swept the size and observed the sense margin and sense current for the 50nm M5 width (Figure 9(b)). It is evident from the plot that the sense margin increases sharply from 50nm to 200nm. After 200nm, improvement in the sense margin saturates. Also, the search current increases by approximately $10\times$ with an increase in the width by 25nm. Therefore, we selected the width of M3/M4 to be 200nm.

3.2. The Impact of TMR on Sense Margin

Figure 10 shows the trend of match current and sense margin versus the width of NMOS M5 for different TMR values. The R_L of MTJ is fixed to 8K (as decided in Section 3.1) for this analysis, and TMR and R_H are selected for low match case search current and higher sense margin. It can be seen that higher TMR ensures a better sense margin and low STTMRAM match current with fixed R_L . It can be seen from the plot that the NMOS width does not affect the STTMRAM current compared to that in the miss case, because the MTJ high resistance R_H dominates the effective NMOS resistance of M3/M4-M5. This also results in low drain voltage at M3/M4 compared to that in

the mismatch case. So the width of NMOS is selected based on the mismatch current drawn from the SL while the TMR is chosen to satisfy the match case conditions. It can be noted that the sense margin benefit of TMR greater than 125% saturates. Hence, we have used $\text{TMR} = 125\%$, which provides less than $45\mu\text{A}$ of match current with a sense margin close to 500mV .

Realization of R_L and TMR: Resistance of MTJ is shown to depend on oxide thickness and surface area of free layer [Shen et al. 2006]. Therefore, by tuning these parameters, it is possible to obtain MTJ resistance of $R_L = 8\text{k}\Omega$. Similarly, it has been experimentally shown that TMR could be improved up to 236% [Shen et al. 2006]. This can be used during design time to ensure $\text{TMR} = 125\%$ for proper functioning of the proposed TCAM.

4. SIMULATION RESULTS OF NOR TCAM CELL

In this section, we present analysis of the proposed TCAM with respect to temperature, voltage and process-variations. We also propose modulating search enable signal and threshold voltage to improve robustness.

4.1. Setup

We used $\text{TMR} = 125\%$ with $R_L = 8\text{k}\Omega$, a 50nm M5 transistor, and 200nm M3/M4 transistors (as discussed in Section 3). MTJ models from Fong et al. [2013] are used with $60\text{nm} \times 60\text{nm} \times 3\text{nm}$ free layer dimension and 0.876nm oxide (MgO) thickness for design simulations. Word sizes of 16, 32, 64, 128, and 256 bits are simulated to analyze the design with respect to process, temperature, and voltage variations.

4.2. Temperature Variation Analysis

Thermal fluctuations result in the critical current and switching time variations in the MTJ, which is modeled in the effective magnetic field in LLG equations [Wang et al. 2014]. The worst-case sense margin, search delay (for 50mV sense margin development), and the Power Delay Product (PDP) per bit search from 10°C to 90°C are shown in Figures 11(a)–(c) for different word sizes. A single bit mismatch is considered for sense margin and search delay as is the worst-case condition. The search delay increases proportionally as the word size due to the increment in the ML interconnect capacitance. As the temperature increases, the rate of ML discharge increases due to lowering of the threshold voltage of the discharge transistors M1/M2. The sense margin decreases with temperature due to ML discharge through the subthreshold leakage current of the discharge transistors in the match case. Therefore, the search delay (for the 50mV sense margin) increases with the temperature. The PDP is proportional to the change in search delay while the operating voltage and the search line current are similar across different temperatures. From Figure 11, it is evident that we obtain a reliable sense margin of greater than 50mV across the range of temperature to a 256-bit word size.

4.3. Voltage Scaling

For this study, the operating voltage is varied from 0.7V to 1.2V to observe the sensitivity of the sense margin, search delay, and PDP per bit search (Figure 12). A 50mV sense margin development time is used to measure the search delay. Below 0.7V , the sense margin of a 256-bit CAM word is less than 50mV . The sense margin and search delay are sensitive to V_{dd} due to lowering of the gate voltage of M1/M2 while their threshold voltages remain fixed. At lower voltages, the M1/M2 transistors fail to turn ON or weakly conduct even during mismatch, degrading the sense margin (especially for wider words). Search delay for a 256-bit TCAM word varies from 124ps at 1.2V to

Fig. 11. (a) Sense margin, (b) search delay, and (c) PDP v/s temperature.

Fig. 12. Voltage scaling from 0.7V to 1.2V; (a) sense margin; (b) search delay in logarithmic scale; and, (c) PDP.

Fig. 13. Distribution of sense margin in (a) TT; (b) SS; and, (c) FF corners.

2.098ns at of 0.7V (search delay is plotted in log10 scale). The increase in the search delay results in sharp increase in the PDP at 0.7V.

4.4. Process Variation Analysis

For process variation analysis, we have considered Fast Fast (FF), Slow Slow (SS), and Typical Typical (TT) corners. We have modeled the process variation in transistors by a widely accepted technique of lumping the variation in channel length, oxide thickness, flat band conditions, and so on, into the threshold voltage of the transistor [Ghosh et al. 2006]. The SS (FF) is simulated by adding (subtracting) 150mV from the nominal threshold voltage. Process variation in the MTJ device is modelled by considering the effects of variation in the MTJ surface area and oxide thickness [Wang et al. 2014]. We have considered process variability in MTJ by varying the MTJ set resistance R_L as normal distribution with a mean of $8k\Omega$ and sigma $\pm 500\Omega$ and TMR variation of 0.1% (variation in surface area and oxide thickness). The worst-case sense margin is plotted for different supply voltages at the TT, SS, and FF corners (Figure 13). It can be observed that the design can provide a reliable sense margin of above 50mV at all corners to 0.75V for 128-bit words or less. The poor sense margin at lower voltages is linked with poor V_{gs} across M1/M2 that keeps the ML precharged even in mismatch conditions.

The 256-bit word fails to provide an adequate sense margin in the FF corner at 1V. This is primarily due to poor $\Delta 2$ (as shown in Figure 6) when V_{TH0} moves down coupled with leakage from the match bits. Therefore, match bits leak in case of a mismatch degrading the sense margin. We propose threshold voltage modulation and SE voltage boosting or underdrive to improve sense margin for a 256-bit word. Furthermore, these techniques will not worsen the reliability of the NMOS device, since thicker oxide (associated with high V_{TH}) and lower gate voltage are expected to be better for reliability such as hot-carrier degradation, Negative Bias Temperature Instability (NBTI), and Time-Dependent Dielectric Breakdown.

Fig. 14. Maximum sense margin variation with a 0mV, 50mV, and 100mV V_{TH} implant at (a) $V_{dd} = 1V$ and (b) $V_{dd} = 850mV$.

4.5. V_{TH} and SE Modulation for Sense Margin Improvement

To solve the poor sense margin, we propose to modulate V_{TH0} , $\Delta 1$, and $\Delta 2$ by exploring threshold voltage modulation of transistor M1/M2 (to tune V_{TH0}) and SE voltage modulation (to tune $\Delta 1$ and $\Delta 2$). Figure 14(a) shows the results at 1V for the three PV corners for a 256-bit word at different SE signal voltages and 0mV, 50mV, and 100mV higher V_{TH} . A change in the gate drive of M3/M4 changes their ON resistance and results in corresponding changes in $\Delta 1$ and $\Delta 2$. It can be noted that the optimum choice of SE can improve the sense margin. Moreover, repositioning of V_{TH0} can improve the sense margin further. Figure 14(b) illustrates the sense margin across three PV corners with V_{TH} implants at a 850mV supply voltage. It can be noted that V_{TH} modulation can improve the worst-case sense margin significantly (FF and SS in this case), even though the sense margin in the TT corner is degraded. The improvement results from decreased match case current through M1/M2 at SS and the reverse effect in miss case at FF. At the same time, lower SE increases the resistance of M3/M4 which in turn increases $\Delta 2$. As expected, the sense margin in FF with the V_{TH} implant is comparable

Fig. 15. Match and miss case match line voltages in 1-, 16-, 32-, and 64-bit NAND-type TCAM words.

to a TT corner without an implant. With a 100mV V_{TH} implant, the design can provide a reliable sense margin of above 40mV in all the PV corners even without SE modulation. A 150mV SE underdrive can improve the sense margin at TT to more than 120mV, and a 250mV SE underdrive can improve the sense margin at FF to more than 50mV. So we employ a positive V_{TH} implant of 100mV and a gate control signal SE under the drive by 150mV to improve performance across all the PV corners. A positive V_{TH} implant is realized by thicker oxide, and a gate under the drive below the highest V_g of the technology node improves the device reliability while improving the performance.

5. NAND TYPE TCAM CELL SIMULATION RESULTS

We simulated single-bit, 8-bit, 16-bit, 32-bit, and 64-bit NAND-type TCAM words and the waveform illustrating the match and miss case states of the match line is shown in the Figure 15. It can be seen from the figure that NAND-type TCAM can provide up to 500mV of sense margin from 1-bit TCAM simulation. It is also observed that the sense margin decreases as the number of bits in the word increase due to the charge sharing of the match line from intermediate nodes between the bits of a word. We have measured the miss case match line voltage with the miss on the farthest bit from the sense amplifiers end to consider the worst-case scenario. The sense margin measured for 16-, 32-, and 64-bit TCAM words are 147mV, 90.5mV, and 33.4mV under nominal conditions. The search delay measured for a minimum SM of 50mV for 16- and 32-bit TCAM words are 1.83ns and 2.72ns, respectively. Sixty-four-bit words have a search delay of 5.45ns for 30mV SM. Search delay is measured as the time required to develop required sense margin on the matchline from the time WL crosses $0.5 \cdot V_{dd}$. The sense margin can be improved by adding a capacitor to the match line, which makes it harder for the match line to get charged by the intermediate node voltages with stray charges in case of a miss. This technique increases the match line power due to an increase in match line capacitance.

The search power in a NAND-type TCAM cell at 0.8V and 1V supply voltage are tabulated in Table IV. The power consumption in NAND TCAM is higher than the proposed NOR TCAM. This is due to additional logic around the NOR-type TCAM cell in the design realization. The search delay and sense margin plot for different word lengths of NAND-type TCAM is as shown in the Figure 16. It can be concluded from the plot that the search delay increases by twofold with the number of bits in the TCAM

Fig. 16. Search delay and maximum sense margin of NAND-type TCAM v/s word length.

Table IV. Power (in μW) Comparison of CMOS and Proposed TCAM

	V_{dd} (V)	Match	Miss	Search "X" from SL, $\overline{\text{SL}} = 0$	Search "X" with $D = \overline{D} = 1$
CMOS	0.8	0.3	2.03	1.03	0.2403
Proposed NOR	0.8	24.84	23.8	0.6	22.39
Proposed NOR	1	43.07	53.3	1.02	41.25
Proposed NAND	0.8	24.5	25.08	20.26	29.08
Proposed NAND	1	54.5	43.75	46.4 ($\text{SL} = \overline{\text{SL}} = 1$)	63.9

word (word length). The maximum sense margin decreases greatly for larger word length beyond 64 bits. Maximum sense margin for 64-bit word is 33.4mV with a search delay of 5.8ns, which is due to the larger resistance offered by the PMOS transistor chain in the match line. We have retained the size of PMOS in the match line same for different word lengths for simplicity of analysis and to alleviate the area overhead in larger words.

6. COMPARATIVE ANALYSIS

In this section, we present the comparative analysis of the proposed NOR and NAND TCAM with respect to CMOS CAM and other spintronic CAMs from the literature.

6.1. Comparison with CMOS TCAM

Conventional TCAM cell consists of 16 transistors while the proposed NOR-type TCAM consists of only 6 NMOS transistors and 2 MTJ bits, which is a 63.5% reduction in the number of transistors. For a power comparison, we implemented the CMOS TCAM and simulated it using a 22nm predictive model. The leakage power of the proposed TCAM is zero, as the power supply can be completely shut off during sleep while SRAM TCAM consumes a considerable amount of standby power. In mostly OFF applications such as the Internet-of-Things and smartphones the proposed TCAM could be very attractive compared to CMOS CAM.

The search power consumption of the proposed TCAM is higher compared to conventional CMOS because of the search line current ($\sim 51\mu\text{A}$ in the case of a mismatch at 1V) drawn to generate a secondary voltage at the drain terminals of M3/M4 that enables the discharge transistors of ML. The search line current can be reduced by selecting MTJ with high R_L and high TMR. The power consumption during the search operation of "1" and "0" bits at 0.8V in STTRAM-based TCAM is observed to be up to 80% higher

Table V. Comparison with Other Spintronic CAMs

Parameter	MTJ-based CAM [Xu et al.]	DWM CAM [Nebashi et al.]	DWM CAM [Zhang et al.]	MTJ-based CAM [Chen et al.]	Proposed NOR CAM	Proposed NAND CAM
Technology	180nm	90nm	65nm	32nm	22nm	22nm
CAM type	BCAM/TCAM	TCAM	TCAM	BCAM	TCAM	TCAM
CAM topology	NOR	NOR	NOR	NOR and NAND	NOR	NAND
Search energy/bit	NA	2.9fJ	12fJ	2.82fJ	4.7fJ	6.39fJ
Area	6T-2MTJ (BCAM), 8T-2MTJ (TCAM)	12T-2MTJ	12T-2MTJ	6T-2MTJ (NOR), 5T-2MTJ (NAND)	6T-2MTJ	9T-2MTJ
Search delay	3.3ns (32-bit)	5ns (128-bits)	2ns (8-bit)	34.4ps (1-bit)	263ps (256-bit)	2.72ns (64-bit)
Ext. write circuit	NA	Yes	Yes	No	No	No

in the worst case (successful search of “1”) compared to NOR-type CMOS TCAM. The power consumption of NOR-type CMOS TCAM and the proposed spintronic TCAM are tabulated in Table IV. The NAND-type TCAM consumes 2–3% more power and 50% more number of transistors (6T v/s 9T) compared to the proposed NOR-type TCAM.

6.2. Comparison with Spintronic CAMs

We compared the proposed TCAM cell performance with the other spintronic TCAM structures proposed so far (Table V). The proposed NOR-type TCAM draws $51\mu\text{A}$ ($39\mu\text{A}$) from the search line during mismatch (match), which is significantly more energy efficient than DWM CAM [Zhang et al. 2012]. NOR-type TCAM has 33.3% fewer transistors compared to MTJ TCAM [Xu et al. 2008] and 50% (25%) fewer transistors than DWM TCAM [Nebashi et al. 2011; Zhang et al. 2012]. The proposed NAND-type TCAM has 12.5% additional transistors compared to the MTJ TCAM [Xu et al. 2008] and 33.3% (44.4%) fewer transistors than DWM TCAM [Nebashi et al. 2011; Zhang et al. 2012]. The BCAM proposed in Xu et al. [2008] requires additional circuitry (NMOS transistor and an MTJ) to configure as a TCAM. In the proposed TCAM data can be written to the bit cell by a conventional current-induced magnetization technique [Fong et al. 2013] and controlling the source line. Therefore, it eliminates the need of external writing circuitry. The NMOS transistor M6 (driven by a “WR” signal) provides the additional current required for write. This is unlike in Xu et al. [2008], which does not provide methods for memory write. The TCAM cells [Xu et al. 2008; Chen et al. 2013] MTJs are integrated into search circuit in series which makes the write operation more complex and erroneous. DWM CAMs [Nebashi et al. 2011; Zhang et al. 2012] use domain wall motion-based write and MTJ sense circuit-based search, which adds area overhead and complexity in memory design. MTJ-based CAM proposed in Matsunaga et al. [2012] also uses four transistors (NMOS and PMOS) and two MTJs, and the sensing is based on the amount of current drawn from the match line by different low and high state resistance offered by the MTJ. The technique fails as the number of bits in a word increases (up to 144-bit words). The memory cell has low tolerance to variations in temperature and low V_{TH} process corners due to leakage in the diode-connected NMOS transistor. With larger word capacitance, the ML increases while the differential current remains the same and thus affects the ML sense margin available. The situation becomes worse with process variation of the diode-connected

NMOS transistor. Also, 2T-2MTJ [Matsunaga et al. 2012], which also exploits the resistance differential and segmented search, has complex memory architecture incorporating the control circuitry, an accumulator to store segmented search results, and segment activation. The additional circuits incur delay and power overhead in the scheme. Overall, the technique is not efficient in terms of delay and power compared to other spintronic CAMs. Although search delay is mentioned in Table V for different word lengths, the search delay reported for the proposed TCAM is for larger words (256 bits). Also, in Chen et al. [2013], it is only 7.5 times the search delay in a single-bit search. The proposed TCAM search delay differentiates by its smaller value for a larger word. The network IP address is 128 bits in the IPv6 protocol [Govindaraj et al. 2012]. For 128 bits the search delay is less than 250ps, which can theoretically support 3GHz to 4GHz search speeds for application in routers. We have used a 60nm×60nm IMA MTJ model that shows the write latency of 4ns with a write energy of 0.69pJ/bit.

7. CONCLUSIONS

We proposed a spintronic TCAM that is promising for zero standby leakage and uses fewer transistors. We conducted a detailed analysis in the presence of process, voltage, and temperature variations for a wide range of word sizes. The proposed design operates with a reliable sense margin up to 128-bit word sizes to 0.7V. We also propose threshold voltage modulation and search enable underdrive to improve the sense margin for 256-bit words. The proposed TCAM has 62.5% fewer transistors compared to conventional CMOS TCAM and 33–50% fewer transistors compared to other spintronic CAMs. The worst-case active leakage power of the NOR TCAM cell is measured to be 0.38nW. We also propose a 9T-2MTJ NAND-type TCAM cell, which has 43.75% fewer transistors compared to conventional TCAM cells. Our proposed NOR TCAM cell has better performance and power metrics compared to a NAND TCAM cell. Our study revealed that NOR TCAM using the proposed approach is better than the NAND TCAM in area, delay, and power. Therefore, it makes practical sense to employ the NOR TCAM in search applications.

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