An Overview of Parallel Processors and Processing

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The processing rate of a computer can be conceived as the volume of the cube(s) enclosed by one or more points in a rectangular coordinate system with three axes denoted by the *clock rate*, the *word width*, and the *number of words*. In other words, the processing rate of a computer can be improved by increasing either the clock rates in the system or the number of bits that can be processed simultaneously. The clock rates can be increased by using high-speed switching devices and circuits and by shortening the propagation time in interconnection lines. Indeed, for the past three decades tremendous progress has been made in device and circuit technology and in miniaturization techniques. It is also a well established practice that groups of bits, called words, are processed simultaneously in most computers so that a higher processing rate can be obtained. However, as improvement in switching devices and miniaturization reaches a limit and as word width is limited by the precision of intended applications, it is obvious that any further significant increase in processing speed can be obtained only by the concurrent processing of a number of words. To this end, various multiple-processor systems have been proposed and constructed. Among these, four specific multiple-processor organizations (associative, parallel, pipeline, and multi-processors) and their processing techniques are surveyed in this special issue of *COMPUTING SURVEYS*. All four of these systems have centralized controls. All four have actually been implemented (built and operated). The impact of recent advances in LSI technology in the design and applications of these systems is evident in the surveys presented.

The first paper, by Yau and Fung, treats associative processors. The development of associative processors is based on the search capabilities of associative memories, which are particularly suitable for nonnumerical data processing. During the first decade of development many experimental associative memory models were built, culminating in the delivery of a 50-bit, 2k-word associative memory by Goodyear Aerospace to the Rome Air Development Center in 1968. (A survey by Hanlon of associative memories and their possible applications appeared in 1966.)* Since it was not feasible to construct large associative memories, the emphasis of associative processor design during the following decade tended to focus on systems which are capable of both arithmetic and fast search operations. A number of associative processors, notably PEPE and STARAN, were constructed. (Several surveys by Parhami, Minker, and Thurber and Wald appeared during this period of development.)* However, as a result of recent advances in LSI technology the design of associative processors has entered a new stage of development aiming at the construction of large-capacity associative processors. For example, both ALAP and ECAM, using large serial storages, are designed with a total system capacity in the range of a billion bits. Also, a new model of the commercially available STARAN computer with a storage capacity of

*Specific references are included in the paper by Yau and Fung [see page 24]

several hundred million bits has been introduced. Such new developments are likely to renew the original interest in applying associative processors to nonnumerical, large database applications. Thus the emphasis of Yau and Fung's paper is on new developments of the last few years, with a brief survey of past associative systems.

The second paper, by Kuck, surveys parallel processors. Associative processors belong to the larger class of parallel processors. Thus both associative and parallel processors have a central control unit, a number of processors, memory modules, I/O devices, and interconnection networks between processors and memories. However, associative processors are developed from the concept of associative search capabilities, and in most designs they involve bit-slice sequential operations. Parallel processors, on the other hand, are usually oriented toward high-speed mathematical computations, and their operations are mostly parallel-by-bits and parallel-by-words. So far there has been only one major parallel processor actually constructed, the ILLIAC IV. Kuck's paper emphasizes the theoretical aspects of parallel processing, so his paper and that of Yau and Fung are complementary in content. A major obstacle in the development of parallel processors is cost. However, the recent introduction of low-cost, large-capacity memory modules and microprocessors is likely to stimulate future development. The remaining system component, interconnection networks between processors and memory modules, is discussed in both papers.

The third paper, by Ramamoorthy and Li, is on pipeline processors. The concept of pipelining also dates back two decades. It is a useful technique, applicable to any computer design whenever there are fixed sequences of operations that occur repeatedly. In contrast to associative and parallel processors, where all active processors execute an identical instruction simultaneously, the processors within a "pipe" perform different operations. The Ramamoorthy and Li survey includes theoretical analysis as well as practical aspects of pipeline processors. The survey also provides descriptions of machines developed recently by Cray and Amdahl.

Multiprocessor systems are surveyed in Enslow's paper, which classifies multiprocessors according to their interconnection schemes. This paper also deals with the required software support for multiprocessors. Readers may be interested in his brief chronology and survey of the characteristics of multiprocessor systems (Chart I and Table I, respectively) as well as in a survey by J. L. Baer of some theoretical aspects of multiprocessing [COMPUTING SURVEYS, 5, 1 (March 1973), page 31].

Several survey papers on computer architecture published in this journal are pertinent to parallel processors and processing. Among these the Special Issue on Computer Systems Architecture (December 1975) is particularly relevant. In addition to the paper by Thurber and Wald already mentioned, the other two papers in the special issue deal with computer system components—one, by Keller, on look-ahead processors and the other, by Anderson and Jensen, on computer interconnections. A paper by Reddi and Feustel briefly surveying various aspects of computer architecture in the June 1976 issue of SURVEYS should also be of interest to readers.