Guest Editorial RAW 2014

The 21st Reconfigurable Architectures Workshop (RAW 2014) was held in Phoenix, Arizona, in May 2014. RAW 2014 was associated with the 28th Annual International Parallel & Distributed Processing Symposium (IPDPS 2014). The workshop is one of the major meetings for researchers to present ideas, results, and ongoing research on both theoretical and practical advances in reconfigurable computing. RAW is sponsored by the IEEE Computer Society Technical Committee on Parallel Processing.

A reconfigurable computing environment is characterized by the ability of underlying hardware architectures or devices to rapidly alter (often on the fly) the functionalities of their components and the interconnection between them to suit the problem at hand. The area has a rich theoretical tradition and wide practical applicability. There are several commercially available reconfigurable platforms (FPGAs and coarse-grained devices) and many modern applications (including embedded systems and HPC) use reconfigurable subsystems. An appropriate mix of theoretical foundations and practical considerations, including algorithms architectures, applications, technologies and tools, is essential to fully exploit the possibilities offered by reconfigurable computing. The Reconfigurable Architectures Workshop aims to provide a forum for creative and productive interaction for researchers and practitioners in the area.

RAW 2014 hosted two invited speakers, Joshua Walstrom, Altera Corporation, and Maya Gokhale, Lawrence Livermore National Lab, who presented the state of the art and discussed directions with “Runtime Reconfiguration in Altera FPGAs” and “Reconfigurable Architectures for Extreme Scale Computing,” respectively. The workshop also featured a panel discussion on reconfigurable computing in the multicore era.

In this special ACM TRETs section, we present extended versions of three of the papers from RAW 2014. These articles have been selected out of the 28 conference papers covering various topics, spanning from reconfigurable architectures and algorithms to systems, tools, and applications. The three selected articles, which we introduce briefly below, also reflect this variety of research areas.

The first of these three articles is by Ali M. Zaidi and David Greaves and is entitled “Value State Flow Graph: A Dataflow Compiler IR for Accelerating Control-Intensive Code in Spatial Hardware.” It describes a hardware-implementable intermediate representation called Value State Flow Graph, which allows the compiler to exploit more instruction-level parallelism and energy-/area-performance tradeoff in control-intensive code that is typical of nonnumeric computations. This expands the scope of FPGA accelerators in general-purpose computation.

The second article by Michael Raitza, Markus Vogt, Christian Hochberger, and Thilo Pionteck is titled “Random Number Generators on FPGAs.” It discusses practical considerations in implementing true random number generators (entropy sources) on FPGA components (digital circuitry, in general). Specifically, it investigates the

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robustness of several ring-oscillator designs under adverse conditions such as power supply tampering and with exposure of the chip to extreme temperatures, magnetic fields, and X-ray. This work has relevance in areas such as cryptography, simulations, and gaming where FPGA-type devices are being employed.

The third article is authored by Osama G. Attia, Kevin R. Townsend, Phillip H. Jones, and Joseph Zambreno and is entitled “A Reconfigurable Architecture for the Detection of Strongly Connected Components.” This work implements strongly connected components (SCC) detection for large-scale (random) graphs (possibly with over a million nodes) on an FPGA-based coprocessor board. The proposed design reduces memory latency associated with irregular memory accesses that are typical in handling such large graphs.

We thank the authors of these articles for their excellent work and the anonymous reviewers for their constructive feedback on these articles. We also acknowledge the support of Steve Wilton (ACM TRETTS Editor-In-Chief), Philip Leong (ACM TRETTS Senior Associate Editor) and David Thomas (ACM TRETTS Information Editor) in making this special section possible.

We hope you enjoy the articles in the RAW 2014 special section and that they serve as useful references in your research as well as an introductory to the versatility and scope of reconfigurable computing.

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