Multiple Combined Write-Read Peripheral Assists in 6T FinFET SRAMs for Low- V_{MIN} IoT and Cognitive Applications

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ABSTRACT

Battery-operated or energy-harvested IoT and cognitive SoCs in modern FinFET processes prefer the use of low- V_{MIN} SRAMs for ultra-low power (ULP) operations. However, the 1:1:1 high-density (HD) FinFET 6T bitcell faces challenges in achieving a lower V_{MIN} across process variation. The 6T bitcell V_{MIN} improves either by increasing the size of the bitcell or by using combinations of peripheral assists (PAs) since a single PA cannot achieve the best V_{MIN} across process variation. State-of-the-art works show some combinations of write and read PAs that lower the V_{MIN} of 6T FinFET SRAMs. However, the better combinations of PA for 14nm HD 6T FinFET SRAMs are unknown. This work compares all the possible dual combinations of PAs and reveals the better ones. We show that in a usual column mux scenario the combination of negative bitline with V_{DD} boosting and V_{DD} collapse with V_{DD} boosting in a proportion of 14% and 6% (total 20%), respectively, maximize the static V_{MIN} improvement close to 191mV for ULP IoT and cognitive applications. We also show that a combination of wordline boosting with negative bitline and wordline boosting with V_{SS} lowering achieve a 150mV and 25mV of dynamic V_{MIN} improvement at the 5GHz frequency for the worst-case write and read corners, respectively, beating other combinations.

Categories and Subject Descriptors

• Hardware→Integrated Circuits→Semiconductor Memory→Static Memory.

Keywords

14nm; Cognitive; IoT; FinFET; Low Power; SRAM; V_{MIN} ; Peripheral assists;

1. INTRODUCTION

This paper examines the combinations of write and read peripheral assists for 14nm 1:1:1 high-density (HD) 6T FinFET SRAMs to minimize the operating V_{MIN} for a 20% of total assists' percentage. Energy-constrained IoT and cognitive applications have stringent energy requirements that force the logic and the SRAM to operate at lower supply voltages. As energy has a quadratic relation with the supply voltage (V_{DD}), scaling down the V_{DD} reduces the energy quadratically for both the logic and SRAMs. However, across process variation, lowering supply voltage poses a risk for SRAMs from the write-ability, readability, and read-stability standpoints. Due to poor write margin (WM)

Figure 1: (a) Conventional 6T bitcell. (b) Waveform illustrations of wordline boosting and negative bitline write assists.

[1], read static noise margin (RSNM) [1], and a degraded half-select issue in a bitline interleaving scenario, the 6T SRAM in a bulk technology is vulnerable to operate at near-threshold or sub-threshold voltages. Although alternative half-select-free [2] bitcells operate in near-threshold supplies, they come with significant area overheads for SRAM core arrays. In scaled FinFET technologies, these issues worsen and the 1:1:1 HD 6T bitcell suffers from poor write-ability and read-stability issues at nominal supply voltages in the worst-case corner. Thus, improving the write and read operations for FinFET SRAMs require techniques, such as sizing the bitcell devices, choosing an alternative bitcell [2] topology, applying peripheral assist [1][3] (PA), etc. Changing the topology or increasing the sizing can improve the write and read operations, but is not a preferred option, as they affect the overall density of the bitcells by trading off the SRAM area and its silicon cost. Moreover, due to the quantized width and length of FinFETs, making the 6T bitcell of the worst-case corner to work at the nominal voltage is quite challenging. To achieve a lower V_{MIN} and better yield for corresponding write and read metrics modern FinFET technologies allow the SRAM designers to either use the number of fins to size the 6T bitcell or PAs as design knobs, which increases the SRAM area and energy consumption. In FinFET technologies, apart from read and write V_{MIN} there is another SRAM metric called data retention voltage (DRV) [1] V_{MIN} , which is usually much lower compared to the write-read V_{MIN} and is not affected by the transient PAs. Assists are widely employed in reducing the SRAM V_{MIN} in energy-constrained designs. Recent works demonstrate single and multiple combined PAs (CPAs) [3], which show promises for lowering the HD 6T FinFET V_{MIN} . Nevertheless, no literature compares these single

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and combined assists for write and read SRAM design metrics for HD 6T FinFET SRAMs. Thus, this work investigates to reveal our findings, whether applying a type of single or combined PAs can improve the static and dynamic V_{MIN} of the FinFET HD 6T bitcell below the nominal supply voltage across process and temperature variations. We organize the rest of the paper into ten sections. Section 2 describes the prior art in PAs. Section 3 and 4 shows the challenges in static and dynamic V_{MIN} of HD 6T FinFET SRAMs. We state our experimental assumptions in section 5 and, section 6 and 7 describe the write-ability and read-stability across various single assists for HD 6T FinFET bitcell. We show the worst-case V_{MIN} and margin improvement in section 8 and 9 using single and combined PAs, respectively. Section 10 documents the static and dynamic V_{MIN} improvements using CPA and we conclude in section 11. In the entire paper, we denote the 1:1:1 HD 6T FinFET bitcell as 6T bitcell unless otherwise specified.

2. Prior Art in Peripheral Assists (PAs)

Peripheral assists (PAs) are a class of circuits that help to improve write-ability, readability, and read-stability of SRAMs. The write assists improve the write-ability by increasing the WM or the magnitude of the write static noise margin (WSNM) of the 6T bitcell. Existing works show that we can improve SRAM write-ability by applying PAs such as wordline (WL) (Figure 1 (a)) boosting (Figure 1(b)) [1], negative bitline (BL) (Figure 1 (a)) (Figure 1(b)) [1], supply (V_{DD}) collapse [1], raising ground (V_{SS}) [1], etc. However, some PAs such as the wordline boosting can degrade the read-stability of 6T bitcells. One can bypass the read-stability issues due to poor RSNM of 6T SRAM bitcell using specific bitcell topologies [4][5][6][7]. Also, we can improve the RSNM using read-stability assists such as WL under-drive [1], V_{DD} boosting [1], $\text{neg-}V_{\text{SS}}$ [1], etc., which have much lower overhead compared to a larger-area alternative bitcell in an array scenario. On the other hand, we can improve the SRAM readability using read assists such as V_{DD} boosting [1], negative- V_{SS} ($\text{neg-}V_{\text{SS}}$) [1], etc. Prior work [8] shows the write and read static margins, V_{DD} , and delay trade-offs of a fixed capacity 6T SRAM across various PAs. The work [8] propose a new combination of negative bitline with V_{DD} boosting for V_{MIN} improvement in 130nm bulk and sub-20nm FinFET technologies. However, this work lack findings on challenges of dynamic V_{MIN} for 6T bitcell and do not compare all possible combinations of write and read assists. Moreover, the work does not assume any constraints on the total voltage swing of the combined PAs, without which the comparisons could have different total percentages of assists or voltage swings. On the other hand, authors in [9] show that for a fixed SRAM capacity and yield condition, the read and write dynamic V_{MIN} , and bit-error-rate vary across degrees of assists and operating frequencies in a 28nm bulk CMOS technology. However, this work lacks findings on how combining write and read PAs would result in V_{MIN} improvement. Therefore, we investigate the challenges of HD 6T SRAM in FinFET technology, across process, temperature, frequency, etc. knobs, and how single and dual combinations of PAs help in lowering V_{MIN} for 6T SRAM.

3. Challenges in Static V_{MIN} for 6T SRAMs

The static V_{MIN} assumes an infinite wordline pulse-width. We observe from simulations that the static write V_{MIN} of HD 6T FinFET SRAM increases with the capacity, and the SF corner is the worst-case. On the other hand, we find that the static read V_{MIN} also increases with the capacity of the SRAM; however, the worst-case corner is FS. Overall, the write V_{MIN} is the worst-case and Figure 2 shows the worst-case corner for the static V_{MIN} as the

Figure 2: Simulated HD 6T FinFET SRAM static V_{MIN} vs. capacity at 27C temperature across process variation (TT= typical NMOS and PMOS, SS=slow NMOS and PMOS, FS=fast NMOS and slow PMOS, SF=slow NMOS and fast PMOS, and FF=fast NMOS and PMOS).

Figure 3: Simulated HD 6T FinFET SRAM static V_{MIN} vs. temperature for a 16kb capacity across process variation.

Table 1: Trends of the worst case corner across temperatures

Temperature(°C)	Worst Case Corner	Change in Static V_{MIN}
-40 - 0	SF	↓
0 - 35	SF	↓
>35	FS	↑

Figure 4: Simulated HD 6T FinFET SRAM static V_{MIN} vs. magnitude of the write or read static noise margin (SNM) for 16kb capacity at 27C temperature across process variation.

SF corner. Figure 3 shows the overall static V_{MIN} across temperature variation, and the observations are summarized in Table 1. The plot portrays that below 35C the SF corner is the worst-case, which indicates the write V_{MIN} dominates. However, above 35C the FS corner becomes the worst-case for the static V_{MIN} , which signifies that the read V_{MIN} is higher at this temperature region. Figure 4 shows an interesting trend across

corners for the overall static V_{MIN} across the magnitude increase of the SNM (WSNM and RSNM) margin. The figure shows that, below 10mV SNM margin, the SF corner has the worst-case V_{MIN} . From 10mV to about 55mV margin, the FS corner has the worst-case V_{MIN} , and beyond 55mV the FF corner has the worst case V_{MIN} . Thus, across capacity, temperature, and process variation we see more than 300mV of V_{MIN} variation which makes the design of 6T HD SRAM a very challenging task that requires careful selection of assists for the reduction of 6T V_{MIN} .

4. Challenges in Dynamic V_{MIN} for 6T SRAMs

The dynamic V_{MIN} assumes a finite wordline pulse-width and is the worst of dynamic write-ability, readability, and read-stability V_{MIN} . We investigate the effects of HD 6T FinFET SRAM input design knobs, such as process, temperature, and frequency on the dynamic V_{MIN} . Usually, at higher clock frequencies the half-select read-stability is much better, so the read-stability V_{MIN} may exclude from the calculation of dynamic V_{MIN} . However, in tens of MHz of clock frequencies or lower, the row and column half-select V_{MIN} s start to dominate the overall SRAM dynamic V_{MIN} and needed to be taken into account. We simulate the dynamic write V_{MIN} across frequency at 27C for 10kb SRAM capacity. We observe that the SF corner is the worst-case for dynamic write V_{MIN} and the overall write V_{MIN} variation is more than 350mV. Moreover, we simulate for dynamic read V_{MIN} across frequencies at 27C for 10kb capacity. We observe that the read V_{MIN} is worst for the SS corner and the total V_{MIN} variation is around 200mV. The overall V_{MIN} for the 6T SRAM is shown in Figure 5 for 27C temperature. We observe that the SF corner has the worst case V_{MIN} due to write, which is closed to the nominal supply voltage (V_{NOM}). Furthermore, beyond 3.5GHz the worst case V_{MIN} surpasses the V_{NOM} . The overall V_{MIN} variation is 350mV across process corners. Figure 6 depicts the temperature trend for SRAM dynamic V_{MIN} at 2GHz for 10kb capacity. We report the overall V_{MIN} variation across temperature to be closed to 300mV. Thus, addressing the large dynamic V_{MIN} variation across frequency and temperature variations for 6T SRAM design is a challenging task, which needs to be addressed.

5. Experimental Assumption and Simulation Setup

We use the usual static metric measurement technique [10] for WSNM and RSNM margin, as well as static write and read V_{MIN} simulations. For the Monte Carlo (MC) simulations, we took 16K points to simulate static write and read V_{MIN} . Due to static DC simulations, we did not incorporate any parasitics in the bitcell. Also, we use negative of WSNM to portray positive values in plots, as WSNM for a successful write is a negative value. On the other hand, for the dynamic simulation, we use 10K MC points and use a parasitic switch in the FinFET models to add equivalent resistance and capacitance in each FinFETs in the 6T HD bitcell. For the combined PAs we limit the total voltage swing of the assist percentages to 20% of the full-scale supply voltage. We assume the array size to be 128 rows X 128 columns and model the dynamic simulation deck using equivalent loading added to the wordline and bitline of the core array. We obtain the static and dynamic V_{MIN} data for 16kb and 10kb memory sizes and interpolate the failure rates using logarithmic interpolation to compute the V_{MIN} across 8kb, 4kb, 2kb and 1kb sizes. Note that we perform all the simulations in a commercial 14nm technology for the 6T HD FinFET bitcell.

Figure 5: Simulated HD 6T FinFET SRAM dynamic V_{MIN} vs. clock frequency at 27C temperature for 10kb SRAM capacity across process variation.

Figure 6: Simulated HD 6T FinFET SRAM dynamic V_{MIN} vs. temperature at 2GHz clock frequency for 10kb SRAM capacity across process variation.

Figure 7: Simulated negative of WSNM vs. supply voltage at the worst-case write corner SF_{-40C} for a 20% of assist across single PAs for HD 6T FinFET bitcell.

Figure 8: Simulated negative of WSNM vs. percentage of PAs at the worst-case corner SF_{-40C} at 0.8V supply voltage across single assists for HD 6T FinFET bitcell.

6. Static Write-ability Margin of 6T SRAMs across Single PAs

In a conventional 6T SRAM bitcell, to perform a write operation, one of the pass-gate NMOS transistors pulls down the internal node of the bitcell. Thus, during a write '0' operation, one of the pass-gate transistors of the 6T bitcell based on ratioed logic fights with the pull-up PMOS transistor to overcome its drive strength. However, in a corner where the pass-gate transistor is weak, and the pull-up transistor is strong, such as the slow NMOS and fast PMOS (SF) corner, the 6T bitcell faces poor write ability. Hence, the SF corner is the worst-case write corner for the 6T SRAM bitcells. Using write PAs one can improve the write-ability of 6T SRAMs. Figure 7 shows a plot of negative WSNM vs. supply voltage across single PAs at the worst-case write corner SF_{-40C} for a 20% of assist. The plot shows that the wordline boost (WLB) write assist improves the WSNM metric the most, and the V_{DD} collapse (VDU) and negative bitline (NBL) are the second most useful write assists for improving the write-ability of 6T HD FinFET bitcells. Although WLB may be the best write assist from WSNM metric, it hampers the read-stability of the row half-selected bitcells in a bitline interleaving scenario. Note that the bitline interleaving technique is widely used to improve on the Soft Error Rate (SER) [11] from sub-atomic particle strike in 6T SRAM bitcells. Thus, it is critical to know what percentage of write assists improve the WSNM without affecting the read-stability. Moreover, the read-stability assists are used to suppress the effect of row half-select issues, but hamper the write operation. Thus, Figure 8 shows the negative WSNM vs. the percentage of PAs to identify the trends and behaviors of write-ability and read-stability single assists at the SF_{0.8V}_{-40C} corner. The plot shows that the WLB, NBL, VDU, and V_{SS} raising (VSR) are write assists and increasing the percentage linearly increases the magnitude of WSNM. On the other hand, wordline under-drive (WLU), V_{DD} boosting (VDB), and negative V_{SS} (NVS) are read-stability assists, as they decrease the magnitude of WSNM with increased assist percentages. Choosing the appropriate assists for improving the SRAM write-ability is a challenging task. Thus, an SRAM designer should carefully choose the write assist techniques as well as the percentage of assists based on the WSNM requirements to meet the write-ability and read-stability specifications.

7. Static Read-stability Margin of 6T SRAMs Across Single PAs

The 6T bitcell read-stability metric (RSNM) depends on the beta-ratio of the pull-down NMOS transistor to the pass-gate NMOS transistor. For a better read-stability during the SRAM read, the drive strength of the pull-down NMOS transistor must be strong enough, compared to the pass-gate NMOS transistor. The higher drive strength of the pull-down NMOS ensures that the voltage drop in the internal node (junction of pass-gate NMOS and pull-down NMOS) keeps below the threshold voltage of the pull-down transistor on the other side of the bitcell. Thus, the worst-case corner for the read-stability would be when the pass-gate NMOS transistor is robust, and the pull-down NMOS transistor is weak, or the pull-up PMOS on the other side is weak. In other words, the corresponding worst-case corner is the fast NMOS and slow PMOS (FS) corner. Using read assists one can improve the read-stability of the 6T SRAMs. Figure 9 shows the plot for RSNM vs. supply voltage at the FS_{85C} corner for 20% assist percentage across various single assists. The plot shows that the VDB and WLU are the best row half-select read-stability assists. Contrary to this, the WLB write assist has the

Figure 9: Simulated RSNM vs. supply voltage at the worst-case read-stability corner FS_{85C} for a 20% of assist across single PAs for HD 6T FinFET bitcell.

Figure 10: Simulated RSNM vs. percentage of PAs at the worst-case read-stability corner FS_{85C} at 0.8V supply voltage across single assists for HD 6T FinFET bitcell.

Figure 11: Simulated worst-case static V_{MIN} of the 6T HD SRAM vs. assist percentages for a 16kb SRAM capacity.

Figure 12: Simulated negative write static noise margin (-WSNM) vs. supply voltage at the SF_{-40C} corner across dual assists using a total of 20% (10% percentage each) assist percentage for HD 6T FinFET bitcell.

worst row half-select read-stability. For the column half-select issue, the NBL write assist has the best read-stability compared to

Figure 13: Simulated negative write static noise margin (-WSNM) vs. dual assist percentage at the SF_-40C corner using 0.8V supply voltage across dual assist combinations.

Table 2: Effects of the write and read combined assist techniques (AT) on write-ability (WR) and read-stability (RS).

AT	WR	RS	AT	WR	RS	CPA V_{MIN} Improvement
WLU	↓	↑	NBL	↑	↑	Minimum
WLU	↓	↑	VDU	↑	↑	Minimum
WLU	↓	↑	VSR	NA	↑	Minimum
WLB	↑	↓	VDB	NA	↑	Moderate
NBL	↑	↑	VDB	NA	↑	Maximum
VDU	↑	↑	VDB	NA	↑	Maximum

Figure 14: Simulated worst-case static V_{MIN} vs. working dual assist percentages for a 16kb SRAM capacity for HD 6T FinFET SRAM V_{MIN} lowering.

Figure 15: Cumulative distribution of 100 chip simulations of dynamic write V_{MIN} across single and dual assist percentages at the SF_27C corner using a total of 20% (10% percentage each) assist percentage for a 16kb capacity of HD 6T FinFET SRAM at the 5GHz clock frequency.

the others. It is crucial to ensure that an SRAM designer chooses the proper percentages of read-stability assist to meet the SRAM specifications. Thus, Figure 10 shows the trends and comparison

Figure 16: Cumulative distribution of 100 chip simulations of dynamic read V_{MIN} across single and dual assist percentages at the SS_-40C corner using a total of 20% (10% percentage each) assist percentage for a 16kb capacity of HD 6T FinFET SRAM at the 5GHz clock frequency.

of assists for RSNM metric for read-stability at the FS_0.8V_85C corner. The plot shows that the percentage increase of write assist degrades the read-stability in a column mux scenario; however, NBL has the best, and VDU and VSR have the second-best column half-select read-stability among all the write assists. On the other hand, WLB has the worst RSNM read-stability magnitude across assist percentages.

8. Worst-case V_{MIN} Improvement Using Single PAs

We simulate the static write V_{MIN} across single assist percentages at the SF_-40C corner. We find that the WLB, VDU, VSR, and NBL improve the write V_{MIN} at the worst-case corner. On the other hand, the VDB and WLU read-stability assists degrade the write V_{MIN} with the increase of assist percentages. We further simulate the static read V_{MIN} across single assist percentage at the worst-case FS_85C corner. We observe that the VDB and WLU are the only assists that improve the read-stability V_{MIN} with increasing assist percentages. Besides, the NBL, VSR, and VDU write assists have the lowest column half-select V_{MIN} that increases slowly with assist percentages. Noticeably, without bitline interleaving, single write and read assists can lower the 6T SRAM V_{MIN} . However, in widely-used bitline interleaving or column mux scenarios, none of the single assists can improve the worst-case V_{MIN} across assist percentages (Figure 11). Improving the worst-case V_{MIN} in column mux scenario requires combinations of write and read assist, those have shown to work in the state-of-the-art. However, it is not shown exhaustively what the potential write-read assist combinations are that would work, and which combination is the best, with the assumption that the total voltage swing of the assists is constant. We investigate the effect of write and read combined PAs to improve the worst case V_{MIN} in the next section.

9. Combined Peripheral Assists (CPA) for SRAM Margin Improvements

As single PAs fail to lower the worst-case 6T V_{MIN} at 14nm technology in the column mux scenario, we investigate all feasible write and read CPAs and their percentages that allow us to reduce the worst-case SRAM V_{MIN} . Figure 12 shows the plot for negative WSNM vs. supply voltage across dual assist combinations at the SF_-40C corner using equal 10% each assist percentages. The plot shows that the combinations WLB + NBL and WLB + VDU are the best that improve the magnitude of WSNM. The second best combinations for strengthening the WSNM are WLB + VSR and NBL + VDU. Figure 13 shows the plot for negative WSNM vs. various dual assist percentage combinations at the SF_0.8V_-40C

corner. The figure shows the better double assist combinations for improving the write-ability (NBL + VSR, NBL + VDU, WLB + NBL, WLB + VDU, and WLB + VSR) and row half-select read stability (WLU + NBL, WLU + VSR, and WLU + VDU). On the other hand, we further simulate for RSNM across supply voltage across and various dual assist percentages at the FS_85C corner using (each assist with 10% strength) a total of 20% assist percentage per combination. We find that the assist combinations NBL + VDU, and NBL + VSR have the best RSNM for column half-select read-stability and WLU + VDB has the best row half-select stability. Similarly, we simulate for RSNM across dual assist percentages with the total assist percentage of 20% at the FS_0.8V_85C corner and find that NBL+VDU and NBL+VSR give the better combinations for improving read-stability.

10. Improvement of SRAM Static and Dynamic V_{MIN} using CPA

Table 2 gives the write and read combinations' (row-wise) effects on write-ability and read-stability metrics indicating the corresponding V_{MIN} savings. Figure 14 shows all valid combinations of write and read assist that allow us to lower the worst-case V_{MIN} . Noticeably, the combinations NBL + VDB (191mV V_{MIN} improvement) and VDU + VDB (175mV V_{MIN} improvement) achieve the lowest V_{MIN} s close to 0.6V using 14%_6% assist combinations. The combinations WLU + NBL, WLU + VDU, and WLU + VSR have relatively higher minima in V_{MIN} across dual assist percentages compared to the NBL + VDB, etc. blends. However, using VDB could have more energy and layout penalty compared to the circuit implementation of NBL or VDU or VSR, as the boosting cap for VDB may be much higher due to higher capacitance in the V_{DD} route. Thus, although the combinations NBL + VDB and VDU + VDB achieve a lower minima in V_{MIN} , they may have higher energy and layout penalties compared to the circuit implementation of the WLU + NBL, etc. combinations.

We also perform 100 chip simulations using 16K Monte Carlo samples for dynamic write and read operations without bitline-interleaving scenarios to capture if this notion of combined assist using a fixed total percentage of voltage swing is capable of lowering the V_{MIN} across assist blends. Figure 15 shows the plot for the cumulative distribution function of the dynamic write V_{MIN} across single and dual combinations of assists at the 5GHz clock frequency, with a total of 20% fixed assist percentage using 10% each for double assists. The plot shows that the combination of WLB + NBL beats all other combinations and achieves 150mV V_{MIN} improvement at the SF_27C corner. On the other hand, Figure 16 shows the plot for the cumulative distribution function of the dynamic readability V_{MIN} across single and dual combinations of assists, with a total of 20% fixed assist percentage using 10% each for double assists. It shows that WLB + NVS has a better cumulative distribution compared to other blends and it improves 25mV of read V_{MIN} across 100 chip simulations at the worst-case SS_-40C corner.

11. Conclusions

6T HD FinFET SRAM design sees challenges from the variations of process, temperature, frequency, and other design parameters, and has more than 300mV of V_{MIN} variation across these design knobs. Without the bitline interleaving scenario, the traditional write and read single assists can improve the V_{MIN} across design parameters. However, in a bitline interleaving scenario, the worst case static V_{MIN} in 6T high-density FinFET SRAMs is above the nominal supply voltage, and none of the

single peripheral assists can improve it. Only selected combinations such as 14%_6% proportion of V_{DD} boosting with wordline boosting, wordline underdrive with V_{DD} collapse, etc. are suitable. Using write and read combined peripheral assists, the overall static V_{MIN} reduces to have a minimum value across double assist percentages. On the other hand, we show that without bitline-interleaving scenarios the 10%_10% combination of wordline boosting with negative bitline beats all other single and dual combinations for high-speed dynamic write V_{MIN} improvement. Thus, selecting the right peripheral assist combinations with appropriate percentages could help improve V_{MIN} lowering in SRAMs, as well as improving the SoC level battery-life in battery operated IoT and cognitive applications.

12. ACKNOWLEDGMENTS

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