Guest Editorial:

ACM JETC Special Issue on New Trends in Nanoelectronic Device, Circuit, and Architecture Design: Part 2

To enable the next generation of computing, advanced and novel circuits and computing architectures need to be developed based on emerging nanoelectronic devices to achieve an order of magnitude improvement in performance. Co-optimizations must be performed across multiple design hierarchies from device to architecture to provide high-performance data sensing, storage, and processing while satisfying the requirements for power efficiency, reliability, and programmability. Emerging technologies when combined with the explosion in the volume of data have created multiple high-impact design challenges. Hence, novel and significant advanced in design methodologies are required to improve design techniques, design efficiency, enhance performance requirements like reliability, and drastically shorten the design period. Security aspects of such designs and design methods need to be explored, as these new challenges expose new security issues. Hence, there is an immediate need to revise the conventional design strategies and further develop new methodologies for implementing the emerging sensing, storage, and computing paradigm.

This special issue focuses on novel device technology and circuit and architecture designs to implement smart, efficient, reliable, and secure sensing, storage, and computing paradigms. The submissions were from various venues such as the following: (1) the IEEE Computer Society Annual Symposium on VLSI (ISVLSI) 2018 at Hong Kong, SAR, and (2) open domains. All the submissions have been reviewed rigorously following the guidelines of the ACM *Journal on Emerging Technologies in Computing Systems (JETC)* through ScholarOne at <https://mc.manuscriptcentral.com/jetc>. The invited reviewers represent expertise in their fields who provided high-quality reviews of the articles. The articles selected through a rigorous review process for this Special Issue are briefly introduced in the rest of this guest editorial.

The new memory and computationally intensive neural network applications such as recent advances in deep neural network demand more than millions of parameters, which significantly challenges the traditional computing hardware. The crossbar array architecture has been considered one of the promising deep learning architectures that shows a significant computing gain over the conventional processors. However, the feasibility of the architecture still requires investigation, especially for the impact of failed cells due to the initialization process of the resistive memory-based crossbar array. Kim et al., in “[Hardware and Software Co-optimization for the Initialization Failure of the ReRAM-based Cross-bar Array](#),” categorize the possible failures and propose hardware implementation that minimizes catastrophic failures.

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Domain-wall memory (DWM) provides high-density on-chip storage and enables energy-efficient computation for deep neural network applications. Samavatian et al., in “[RNNFast: An Accelerator for Recurrent Neural Networks Using Domain-wall Memory](#),” present a very efficient and highly scalable hardware accelerator for recurrent neural networks (RNNs), which takes the advantages of DWM’s high density and low read/write energy and, at the same time, utilizes the sequential nature of input/weight processing of RNNs to mitigate the downside of DWM on the linear (rather than constant) data access time to achieve significant performance and energy improvement compared with GPU.

Neuromorphic computing based on spiking neural network (SNN) has emerged as a promising artificial neural network with its very high energy efficiency. However, it is inefficient for SNN to perform the convolution based on frames due to the redundant information. Neuromorphic event-based sensors with their output based on AER events are promising to address the problems. Kang et al., in “[ASIE: An Asynchronous SNN Inference Engine for AER Events Processing](#),” present an SNN hardware inference engine based on an asynchronous Processing Element (PE) array for AER events processing and distributed storage of the membrane potential in the PE to achieve a dramatically reduced power consumption per PE.

Computing-in-memory (CIM) is proposed to alleviate the processor-memory data transfer bottleneck in traditional von-Neumann architectures, and spintronics-based magnetic memory has demonstrated many advantages in implementing CIM paradigm. Since hardware security has become one of the major concerns in circuit designs besides performance, for the first time, Wang et al., in “[Hardware Security in Spin-based Computing-in-memory: Analysis, Exploits, and Mitigation Techniques](#),” investigate the spin-based CIM architecture from a security perspective.

The last article also enhances the security of Internet-of-Things (IoT) networks leveraging the benefits of emerging memristors. Networks of low-power IoT may not always have enough computing power to support mainstream cryptographic schemes. Such schemes also consume computing power that can be exposed to side channel attacks. Cambou et al., in “[Cryptography with Analog Scheme Using Memristors](#),” describe a method leveraging the physical properties of memristors to generate cipher text and decrypt them with very low power, which is below observable level through differential power analysis.

Finally, we thank the authors for their patience and dedication at all stages of the review process. Each manuscript was assigned at least three reviewers and has undergone multiple rounds of peer review. The team of guest editors sincerely hope that this special issue will be an important reading for contemporary researchers worldwide. The guest editors sincerely acknowledge the current and past Editors-in-Chief of *JETC*, Drs. Ramesh Karri and Yuan Xie, and the whole editorial team. The guest editors are extremely thankful to the reviewers for their timely reviews of the submitted manuscripts.

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