AN EXPERIMENTAL DISTRIBUTED SWITCHING
SYSTEM TO HANDLE BURSTY COMPUTER TRAFFIC

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ABSTRACT

An experimental switching system has been built using commercially available integrated semiconductors to switch data. Data messages to be handled by the system may vary in bit rate (100 bits/sec - 4×10^6 bits/sec), message length, and rate of message occurrence.

The system uses a synchronous transmission facility with a crystal stabilized clock rate of approximately 6 MHz. The signalling format chosen facilitates data interchange between a number of similar small sequential machines that share a common transmission facility. Efficient data transmission over common carrier systems requires a change in signal format at the channel inputs.

The transmission system is arranged in the form of a closed loop. Control is passed from one machine to the next via the transmission system and passed down the line immediately if the machine receiving control does not require transmission time. The individual machines communicate with one another

using a set of 16 opcodes (Opcodes). Initial handshaking and subsequent communications between machines is accomplished using the set of 16 codes.

A loop supervisor is presently in the form of a DDP 516 Honeywell computer. In the operating system, this functions to translate ASCII inputs to one of the 16 efficient communication codes. This function will be replaced in each terminal by a read only memory. The loop supervisor will then perform primarily a maintenance function. It will seize control in the event of loop failure and insure against traffic overflow. It will not be concerned with the handshaking involved in setting up calls, nor with the data to be transmitted between conversing stations.

The system was constructed without a common control (a common processor to handle the setting up of calls) to avoid high "getting started costs". The feasibility of a completely distributed message-with-address switching system using a shared, high bit rate, closed loop transmission facility has been established. The complexity of the terminal sequential machine required and the opcode set required have been determined. An analytical traffic study has not yet been performed.

Systems involving interconnected loops are discussed briefly; however, the traffic handling capacity of such systems must be analyzed to determine the memory requirements at the junction points. This paper is concerned primarily with the detailed organization of a single loop.