Closing the gap between analog and digital

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Digitally Assisted Analog Integrated Circuits

In past decades, “Moore’s law”¹ has governed the revolution in microelectronics. Through continuous advancements in device and fabrication technology, the industry has maintained exponential progress rates in transistor miniaturization and integration density. As a result, microchips have become cheaper, faster, more complex, and more power efficient.

We will show, however, that digital performance metrics have grown significantly faster than corresponding measures for analog circuits, especially ADCs (analog-to-digital converters). Since most DSP (digital signal processor) projects depend on A/D conversion in the interfaces, this growing disparity in relative performance increase has the potential to threaten the rate of progress of DSP hardware.

Much of the performance gain in digital hardware can be traced to corresponding advances in integrated circuit technology. For example, over the past 30 years we have witnessed a steady decrease in transistor channel length by two orders of magnitude from 10 μ m in 1970 to less than 0.1 μ m today. While this reduction of feature size benefits analog and digital circuits alike, overall analog

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circuit performance is compromised by other trends such as reduced supply voltages.

Figure 1 shows the relative performance of microprocessors and analog-to-digital converters over the last 15 years. While analog and digital system performance increases exponentially over time, microprocessor performance increased more than a thousandfold compared with an increase of only 10 times for ADCs. As the relative performance gap widens, applications such as digital audio, video, and RF (radio frequency) communication are increasingly limited not by the available digital processing power, but by their analog interfaces.

The digitally assisted analog circuits discussed in this article avoid such trade-offs by delegating analog precision requirements to a digital processor. The relaxed analog requirements translate into improved metrics such as reduced power dissipation or increased speed. Key to this approach is a statistical system identification technique that continuously monitors analog imperfections. Judicious selection of the algorithms employed in the digital processor translates into a negligible area and power penalty from the DSP that further benefits from the continued technology scaling.

ANALOG CIRCUITS

Despite the success of digital computing, analog interfaces

are still needed. In fact, as computing power increases, digital processors need more sophisticated analog circuits to interface with the real world. Figure 2 shows a variety of applications and their interface requirements. For example, digital audio demands analog interfaces with at least 16-bit resolution and operating at up to 100 kHz to convert signals from microphones and other sources to a digital representation. Likewise, DACs (digital-to-analog converters) are used to render the digital data stream to an amplifier and speaker for listening.

The benefits of digital processing and storing audio signals are obvious but contingent on the availability of powerful ADC and DAC interfaces. Such converters are also used in hard-disk drives (HDDs), where sophisticated digital processing replaced simpler analog algorithms to increase the achievable density significantly. Again, although key signal processing functions were relegated from the analog to the digital domain, the challenge shifted for the analog designer to provide converters with a hundreds-of-MHz sampling rate.

With the increasing trend toward battery-powered devices, power dissipation is an important consideration when choosing an ADC. In most portable applications the power budget for an ADC is limited to a fraction of a watt. As shown in figure 2, this dictates a very strict upper limit on performance that depends only weakly on technology. Power dissipation is a showstopper for an increasing number of otherwise attractive applications, such as so-called "software radios." These devices use very high-performance ADCs to directly convert the signal at the antenna of, say, a cellular phone. The demodulation is then performed by a digital processor, which can be reprogrammed easily when standards change. Unfortunately,

a full-featured software radio calls for converters with 16-bit or better precision operating at speeds in excess of 1 GHz. Even if such a converter could somehow be built, its power dissipation of several hundred watts would render it useless in most applications.

In all these applications, analog circuits play a key role determining functionality and feasibility. Without innovations to reduce the large and grow-

ing performance gap between analog and digital circuits, analog circuit capabilities are threatening to become the bottleneck in overall system performance.

ANALOG CIRCUIT DESIGN TRADE-OFFS

Reduced feature size combined with lower supply voltage are the key technology drivers resulting in reduced cost, higher speed, and lower power consumption of digital integrated circuits. For analog circuits, scaling is a mixed blessing. Unlike digital circuits, analog functions are constrained by electronic noise and accuracy requirements, factors that only conditionally benefit from technology scaling and can even deteriorate for very low supply voltages. The result is a complex trade-off, and the net benefit of technology scaling in analog circuits is usually a strong function of implementation and architecture.

Analog circuit design trades speed and precision requirements for power dissipation. While power tends to grow linearly with speed, its relation to precision constraints is far more complex. From a general perspective, precision can be subdivided into three main components. The first and most fundamental limit in accuracy is given by the thermal noise of circuit elements. For example, the available signal headroom and the so-called thermal or “ kT/C noise”² determine the dynamic range in an analog sampled data circuit.

In precision analog circuits, typically those with equivalent resolution of 12 bits or more, the noise-power trade-off is extremely steep: Reducing the standard deviation of the noise by a factor of two requires quadrupling the effective capacitance in the circuit. At constant speed, this necessitates a fourfold increase in transconductance, and hence a 4x increase in power dissipation. In other words, the addition of a single bit to a precision ADC can increase power dissipation up to fourfold. In comparison, the power dissipation of a digital circuit increases only slightly faster than linearly with word length. Power, supply voltage, and capacitor area constraints further limit the maximum achievable analog circuit resolution to 18 to 20 bits in current integrated

circuit technologies. Additional supply voltage reductions may reduce this bound further.

In circuits that are limited by component matching, increasing the precision also translates into a power penalty. To first order, matching accuracy is inversely proportional to component area.³ Therefore, additional precision requires larger components with larger capacitance and a resulting net increase in power dissipation. In contrast to thermal noise, however, matching errors are not fundamental in the sense that they can be addressed without necessarily increasing component size. In many situations, it is possible to overcome matching errors using some form of trimming or calibration. In state-of-the-art ADCs, digital correction and calibration techniques^{4,5} are routinely used both to avoid a matching-induced power penalty and to improve accuracy beyond technology limits.

A third and significant challenge in precise analog signal processing arises from the need for highly linear amplification. In most electronic circuits, precisely linear operation is achieved by using high-gain amplifiers in a negative feedback loop configuration. In some sense, the use of electronic feedback parallels the approach of increasing component size to minimize mismatch. Achieving sufficient gain usually necessitates the use of complex amplifiers that tend to be suboptimal in terms of speed and noise. Just as in the case of mismatch, however, distortion and gain inaccuracy limitations are not fundamental. Resulting errors can be compensated upstream or downstream, preferably through some digital compensation mechanism as well.

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From this point of view, it is most interesting to investigate the potential advantage and power savings that are possible by lifting linearity requirements in analog amplifiers.

DIGITALLY ASSISTED ANALOG CIRCUITS

Analog circuits can take advantage of the high performance of scaled digital circuits by delegating critical design constraints to a digital processor. The potential advantage of such "digital assistance" has been recognized and documented in numerous publications on the subject.^{6, 7, 8, 9, 10, 11, 12, 13} For example, converters routinely use digital circuits for canceling offset voltages. An even more significant and previously unexploited advantage results from removing the linearity constraint from an analog circuit. For example, the mapping from voltage to digital codes in an ADC should be perfectly linear. As pointed out in the previous section, this constraint adds significant complexity and power dissipation to the analog design that could be saved in the digitally assisted solution.

Provided the converter has sufficient resolution, a digital processor could in principle map the nonlinearly

distorted digital converter output to the correct codes using a simple remapping. In a modern process the size and power penalty from the added digital circuits is minimal compared with the power saved by the simpler analog circuits. An ADC serves as a vehicle to substantiate this claim.

PIPELINED ADCS

Pipelined converters have become the predominant topology for ADC resolutions of 8 to 14 bits and conversion rates of 10 to 200 megasamples per second (MS/s). Applications include disk drives, digital cameras, wireless receivers, and base stations, just to name a few. Pipelined converters are available as stand-alone parts but are more often embedded in mixed analog-digital chips.

Figure 3 shows a conceptual block diagram of this converter topology. Several converter stages are cascaded and process the analog input sequentially, analogous to flip-flops propagating a bit stream in a digital shift register.

Each stage performs a sample and hold operation and a coarse A/D conversion. The local quantization result is converted back into analog form and used to compute the error in the coarse digital approximation D . The locally computed and amplified quantization error, usually called the residuum (V_{res}), propagates through subsequent stages, which resolve less significant digital information of the initial input sample. After the signal has passed through all stages, the sub-quantization results are combined to yield the final digital output word.

The main advantage of this architecture is that because

of stage pipelining, its throughput rate is set by the time needed to perform a single sub-A/D and D/A conversion. The fact that the signal needs to propagate through all stages until the final conversion result becomes available results only in conversion latency, which is tolerable in many signal-processing applications.

The architecture is inherently tolerant of errors in the sub-ADCs, provided that the DACs and amplifiers are accurate. Conventional implementations use electronic

feedback to meet the amplifier precision requirements. As discussed previously, however, the cost of this desirable feature is an excessive voltage gain requirement. In the front end of high-resolution pipelines,¹⁴ complicated multistage amplifiers with open-loop gain of greater than 100,000 are often needed to meet the stringent accuracy requirements. This results in excessive power dissipation. As a result, residue amplifiers dominate the power dissipation of pipelined ADCs, with a typical contribution of 40 to 70 percent of the total ADC power.

AMPLIFIER DESIGN

Replacing precision residue amplifiers with simple open-loop stages and correcting for the resulting errors digitally is an excellent opportunity to mitigate both of the above-mentioned issues. Figure 4 compares a typical high-gain two-stage amplifier with the proposed single-stage solution. The high-gain amplifier uses a combination of two

cascaded gain stages and a helper amplifier to achieve the required voltage gain of more than 100,000. The proposed solution consists of a simple resistively loaded differential pair.

The advantage of the low-gain amplifier is not limited to the obviously reduced transistor count and design complexity. Simply counting the number of current-carrying branches suggests reduced power dissipation, as does the elimination of the helper amplifiers. Reduced noise and increased signal range at the output of the single-stage amplifier translate into a further significant reduction of power dissipation for a given operating speed.

When applied to the first stage of a 12-bit 75-MS/s pipelined ADC, the power dissipation of the open-loop amplifier was a third of that of the high-gain solution.

STATISTICAL PARAMETER ESTIMATION

Open-loop amplification results in significantly reduced

power dissipation or higher sampling speed but depends on a digital postprocessor to correct amplifier nonlinearity. INL (integral nonlinearity) measures the deviation of the ADC characteristic from a straight line normalized to converter resolution. Many applications demand linearity within one quantizer step or better. Figure 5 shows the measured nonlinearity for a converter with open-loop amplification.

While resulting in significantly reduced power dissipation, open-loop amplification introduces an intolerable amount of nonlinearity. This error can be corrected digitally, but doing so requires accurate correction parameters. Unfortunately, the error signature and, hence, the correction parameters, are different for every part. Moreover, they depend on the temperature. It is

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therefore imperative that the correction parameters are continuously measured by the converter itself.

One solution is to disconnect the converter from the input signal periodically and instead convert a known calibration signal. The digital postprocessor then calculates the correction parameters from the deviations of the converted signal and the expected value. Though simple, this solution has several drawbacks. In many applications, the converter must be available continuously and peri-

odic recalibration sequences are not acceptable. A second challenge is the need to generate an accurate calibration signal, thereby reintroducing the need for analog circuit accuracy, which this approach tries to avoid.

Instead, a statistical approach is used that employs the input signal of the converter itself to extract the calibration information without interrupting the operation of the converter. Figure 6 illustrates the concept: Nonlinearity in a converter can be detected easily by comparing the change ΔD_{out} at the output with a fixed input voltage step ΔV_{in} for different input voltages V_a and V_b . Deviations of the two step heights indicate nonlinearity. A feedback loop updates the correction parameters to minimize the difference of the output step height.

The actual implementation cannot rely on a known input step ΔV_{in} . Instead, it switches randomly between V_a and V_b and counts the number of occurrences in each case for which the converted output is less than a particular threshold. Since the random control signal and the unknown converter input are uncorrelated, the two counts will be equal if the converter is linear. Of course, keeping track of these counts with the digital postprocessor is straightforward.¹⁵

Figure 7 shows the integral nonlinearity of the converter again with digital correction enabled. The INL drops to less than one converter step size, comparable to the performance achieved with the high-gain amplifier, albeit at lower power dissipation.

SHIFT TOWARD ANALOG-DIGITAL CODESIGN

Technology scaling has resulted in a more than two-orders-of-magnitude relative performance gap between analog and digital circuit performance over two decades.

Although analog circuits benefit from scaling, the advantage is partially offset by reduced power supply voltage and intrinsic transistor voltage gain. Since overall system functionality depends on analog and digital circuit performance, analog circuits increasingly determine overall capabilities.

Accuracy requirements are the most prominent and challenging difference between analog and

digital circuits and a significant factor in the relatively lower performance of analog circuits. Digitally assisted analog circuits avoid the disadvantages of technology scaling by delegating accuracy requirements to a digital processor. The relaxed analog circuit constraints translate into higher overall system performance, such as reduced power dissipation or increased circuit speed.

Demonstrated with a state-of-the-art ADC, the concept is applicable to a broad class of mixed analog-digital circuits. For example, digital processing can be used to linearize the power amplifiers or entire communications channels. The approach exploits the vast processing power of modern digital devices that implement functions at negligible cost, which only recently were unfeasible to realize. This suggests a paradigm shift from high-precision analog circuits to mixed analog and digital solutions capable of more broadly taking advantage of modern integrated circuits technology. Q

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