A CONSIDERATION OF THE NUMBER OF HORIZONTAL GRIDS USED IN THE ROUTING OF A MASTERSLICE LAYOUT

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Abstract

In the masterslice LSI, since the wiring area is fixed, local wiring congestion is likely to occur, which may cause the occurrence of some wiring nets to be unroutable. If the number of grids used in the routing can be accurately predicted before the wire routing, it is possible to reduce greatly the occurrence of wiring nets to be unroutable.

This paper describes that the minimum number of horizontal grids used in a routing can be theoretically proved under the condition that the net interconnecting n terminals has at most n sites for trunk partitions. The experimental results on a masterslice LSI with 624 gate cells are in good agreement with the theoretical results.

1. Introduction

The masterslice method seems to be on the verge of explosive growth for moderate volume applications of semicustom LSI circuits. In this method large numbers of gate cells and input/output buffer cells with certain logic functions are prepared and the goal logic circuit is realized by connecting those cells. In order to achieve error free-design and a further reduction of design cost and turn around time, automated procedure has been used extensively in the wire routing design of masterslice LSI.

Since the wiring area is fixed in masterslice layout, local wiring congestion is likely to occur, which may cause the occurrence of some wiring nets to be unroutable. If the number of grids used in the routing can be accurately predicted before the wire routing, it is possible to predict whether or not the wire routing is completed and to reduce greatly the occurrence of wiring nets to be unroutable.

Recently, many works¹⁻³ have been reported on the minimum width routing of two cell-rows where the minimum width is the smallest possible number of horizontal grids in which the routing is accomplished. And T.Kawamoto⁴ obtained the number of horizontal grids used in the minimum width routing of N cell-rows (N : number of cell-rows), and presented the algorithm to complete the required routing by the minimum width. A number of trunk partitions, however, must often be introduced for completing the required routing by the minimum width. A trunk is defined as the horizontal wire segment and each trunk partition divides one trunk into two trunks. Since the dogleg router^{5,6} will introduce trunk partitions only at a terminal posi-

tion for the net, the routing program which employs the routing algorithm with two stages of global routing and channel routing based on the dogleg algorithm, will be unable to complete the required routing by the minimum width.

The next section describes that an interconnection requirement D of N cell-rows is defined in a masterslice LSI chip shown in Fig.1. In the following sections 3 and 4, we restrict the number of trunk partitions and consider the minimum number of horizontal grids used in the routing for the interconnection requirement D . The section 5 presents experimental results of a masterslice LSI with 624 gate cells.

2. Formulation of the Wire Routing Problem

Our model and formulation of the wire routing problem in a masterslice LSI are given as follows.

(1) Parallel horizontal cell-rows on the LSI chip shown in Fig.1 are regularly arranged where the cell-row is treated as the row of terminals. Each terminal is given the number s over integers $0, 1, 2, \dots, S$ where S is the number of nets. All the terminals of the number s must be interconnected by the net which is denoted by W_s . But a terminal assigned with 0, which we call the unused terminal, is the one that is connected with no net.

(2) An intervening wiring area between two adjacent cell-rows is called a horizontal channel. There are two layers for the interconnections; the interconnecting nets must be laid in horizontal channels vertically on one layer and horizontally on another layer on the regularly spaced grids. Wire segments of one net laid on the horizontal (vertical) grids are called the horizontal (vertical) wire segments. Two wire segments of two distinct nets can not overlap on the same grids, and they can cross only when one is on the vertical grid and the other on the horizontal grid. Two wire segments of a net may be connected through a through-hole at the place where they meet with.

(3) The terminals can be connected with nets from above and below. Vertical wirings are possible on the vertical grids corresponding to the unused terminals.

(4) Let N be the number of cell-rows on the LSI chip and let P be the number of terminals arranged in each cell-row. An interconnection requirement D , abbreviated as requirement, is represented as follows.

$$D = [T_1, T_2, \dots, T_N, L, R] \quad (1)$$

T_i represents the ordered alignment of terminals

on the i th cell-row, and is given as

$$T_i = (t_{i1}, t_{i2}, \dots, t_{ip}) \quad t_{ij} \in \{0, 1, \dots, S\} \quad (2)$$

L and R represent the sets of nets interconnected to the terminals on left and right side of the LSI chip, respectively.

(5) For a given requirement D , the terminals $t_{1j}, t_{2j}, \dots, t_{Nj}$ lie always on the same vertical grid. This vertical grid is called the j th vertical grid and denoted by v_j .

We conduct a theoretical investigation of the wire routing problem under the following assumption.

(1) A non-terminal vertical grid, abbreviated as non-terminal grid, is defined as a vertical grid whose corresponding N terminals in N cell-rows are all unused terminals as shown in Fig.2. Any number of non-terminal grids can be inserted between vertical grids.

(2) Interconnections of nets to the terminals on left and right sides of the LSI chip are made with using the vertical channels prepared there, but these interconnections are here ignored.

(3) The net interconnecting only the terminals in a equivalence class of the equivalence relation $\sim$ defined in Definition 2 is one satisfying the following conditions.

(i) The net interconnects only the terminals on a vertical grid v_j .

(ii) The routing of the net is completed on the vertical grid v_j without using horizontal grids.

This net is here ignored. We assume that this net has been routed on the vertical grid.

The assumption (1) seems to give a certain restriction to our results in practical sense. In the masterslice LSI considered, many terminals are unused as logic terminals so that vertical wirings are possible on the vertical grids corresponding to these unused terminals. Most of the nets are the nets interconnecting terminals in the one same cell-row and the nets interconnecting terminals in the two adjacent cell-rows. In this case our results are effective under the assumption that no insertion of non-terminal grid is permitted. This is shown in the section 5.

Fig. 1 Chip structure of LSI.

3. Definition of the Maximum Crossing Numbers

Two kinds of the maximum crossing numbers C_{NM} and C_{TM} , called the maximum numbers of the crossing nets and the crossing trunks, respectively, are defined for a given requirement D .

[DEFINITION 1] For a given requirement D , $C_N(j)$ is the set of all nets that cross the vertical grid v_j at least once in any routing, or that terminate at a terminal on the vertical grid v_j . The maximum crossing number C_{NM} is defined as follows.

$$C_{NM} = \max_{1 \leq j \leq P} |C_N(j)| \quad (3) \quad (\text{END})$$

[DEFINITION 2] For a given requirement D , let t_{ij} and t_{kj} be two terminals on a vertical grid v_j . t_{ij} stands in the binary relation $\sim$ to t_{kj} (symbolically $t_{ij} \sim t_{kj}$), if t_{ij} and t_{kj} satisfy the following two conditions.

(1) $t_{ij} = t_{kj} > 0$

(2) $t_{lj} = 0$ or $t_{lj} = t_{ij}$ for every l such that $i \leq l \leq k$ or $k \leq l \leq i$. (END)

The binary relation $\sim$ is the equivalence relation. Let E_j be the set of all the terminals laid on the vertical grid v_j and used as logic terminals, where the set E_j does not contain the terminals to which the net shown in the assumption (3) in the preceding section is connected. The equivalence relation $\sim$ partitions the set E_j into the disjoint equivalence classes. The set of the equivalence classes is said to be the quotient set of E_j induced by $\sim$ and denoted by $E_j/\sim$.

[EXAMPLE 1] If two terminals laid on the vertical grid v_j are given the same numbers and can be interconnected on the vertical grid v_j , the equivalence

Fig. 2 Equivalence relation $\sim$.

Fig. 3 Interconnection requirement D of example 2.

relation $\sim$ holds between the two terminals. For example, in Fig.2, $t_{2j} \sim t_{3j}$, but the relation $\sim$ does not hold between t_{1j} and t_{4j} . The relation $\sim$ partitions the set $E_j = \{t_{1j}, t_{2j}, t_{3j}, t_{4j}\}$ into the three equivalence classes and $|E_j/\sim| = 3$ as shown in Fig.2. (END)

[DEFINITION 3] For a given requirement D, $A(j)$ is the set of all nets that cross the vertical grid v_j at least once in any routing, and that do not terminate at any terminal on the vertical grid v_j . Then, $C_T(j)$ is defined by

$$C_T(j) = |A(j)| + |E_j/\sim| \quad (4)$$

The maximum crossing number C_{TM} is defined as follows.

$$C_{TM} = \max_{1 \leq j \leq P} C_T(j) \quad (5)$$

[LEMMA 1] For a given requirement D, the crossing numbers C_{NM} and C_{TM} satisfy

$$C_{NM} \leq C_{TM} \leq C_{NM} + N - 2 \quad (6)$$

[PROOF] By the definition of $C_N(j)$, $A(j)$ and $E_j/\sim$, $0 \leq |C_N(j)| - |A(j)| \leq |E_j/\sim| \leq N$

If $|E_j/\sim| = N$, $|C_N(j)| - |A(j)| \geq 2$. If $|C_N(j)| - |A(j)| \leq 1$, $|E_j/\sim| \leq 1$. Thus $0 \leq |E_j/\sim| + |A(j)| - |C_N(j)| \leq N - 2$

Therefore,

$$C_{NM} \leq C_{TM} \leq C_{NM} + N - 2$$

where $C_{TM} = C_{NM} + N - 2$ if and only if $t_{1j} = t_{3j} = \dots > 0$ and $t_{2j} = t_{4j} = \dots > 0$ ($t_{1j} \neq t_{2j}$) on the vertical grid v_j such that $C_N(j) = C_{NM}$. (Q.E.D)

[EXAMPLE 2] Consider the requirement $D = [T_1, T_2, T_3, T_4, L, R]$

$$T_1 = (3, 4, 4, 0, 5)$$

$$T_2 = (2, 1, 2, 5, 1) \quad L = \{W_3\}$$

$$T_3 = (1, 2, 1, 0, 2) \quad R = \{W_5\}$$

$$T_4 = (3, 3, 4, 4, 4)$$

This is illustrated in Fig.3. $|E_j/\sim|$ and $A(j)$ are shown as follows.

$$|E_j/\sim| = \begin{cases} 4 & \text{for } j=1, 2, 3, 5 \\ 2 & \text{for } j=4 \end{cases}$$

$$A(j) = \begin{cases} \emptyset & \text{for } j=1, 2, 3, 5 \\ \{W_1, W_2\} & \text{for } j=4 \end{cases}$$

Therefore, the crossing numbers C_{NM} and C_{TM} are shown as follows.

Fig. 4 A routing by the minimum width.

$$C_N(1) = \{W_1, W_2, W_3\}$$

$$C_T(1) = 4$$

$$C_N(2) = \{W_1, W_2, W_3, W_4\}$$

$$C_T(2) = 4$$

$$C_N(3) = \{W_1, W_2, W_4\}$$

$$C_T(3) = 4$$

$$C_N(4) = \{W_1, W_2, W_4, W_5\}$$

$$C_T(4) = 4$$

$$C_N(5) = \{W_1, W_2, W_4, W_5\}$$

$$C_T(5) = 4$$

$$C_{NM} = \max_{1 \leq j \leq 5} |C_N(j)| = 4 \quad C_{TM} = \max_{1 \leq j \leq 5} C_T(j) = 4$$

An example of a routing for the requirement D is shown in Fig.4. C_{TM} horizontal grids are used in it. (END)

4. The Number of Horizontal Grids Used in a Routing

This section is devoted to theoretical consideration on the number of horizontal grids used in a routing. The following Theorem 1 was proved by T.Kawamoto⁴.

[THEOREM 1] For a given requirement D, the minimum width is C_{TM} or $C_{TM} + 1$ where $N \leq C_{TM}$. (END)

It is easily verified that Theorem 1 holds in our model. Suppose a requirement D is given. Take two adjacent vertical grids v_j and v_{j+1} ($j=1, 2, \dots, P-1$). See an illustrative example shown in Fig.2. On the vertical grid v_j , place both an intermediate terminal² of the net corresponding to the representative of each equivalence class in $E_j/\sim$ and an intermediate terminal of each member of $A(j)$. Likewise on the vertical grid v_{j+1} , place the corresponding intermediate terminals. These intermediate terminals can be placed each on one intersection point of horizontal and vertical grids within upper C_{TM} horizontal grids. Each terminal laid on v_j and v_{j+1} is connected to the corresponding intermediate terminal as shown in Fig.2. It is possible to interconnect the intermediate terminals on v_j and v_{j+1} by using C_{TM} horizontal grids and sometimes one added horizontal grid^{2,4}. Combining these interconnections of the intermediate terminals on v_j and v_{j+1} , the whole circuit will be obtained. Thus Theorem 1 holds in our model.

For a given requirement D , a number of trunk partitions must often be introduced in order to complete the routing by the minimum width proved in Theorem 1 (e.g. see net W_1 in Fig.4). Hence, as mentioned before, the general routing program which employs the routing algorithm composed of two stages, global and channel routings⁵⁻⁷, will be unable to complete the required routing by the minimum width.

Consequently, the number of trunk partitions is restricted in that a net interconnecting n terminals, called the n -terminal net⁶, has at most n sites for trunk partitions, so as for the general routing program to be able to route the net. If n trunk partitions are introduced in a net, the net consists of $n+1$ horizontal wire segments as shown in Fig.5. An immediate consequence of this restriction is that the routing will, in general, be unable to be completed by the minimum width as shown in the example of Fig.4.

[THEOREM 2] The number of trunk partitions is restricted in that n -terminal nets have at most n sites for trunk partitions. If at most $C_{NM}+N-1$ horizontal grids are available for a given requirement D , the routing can be completed.

[PROOF] It suffices to verify that the required routing can be completed by using $C_{NM}+N-1$ horizontal

Fig. 5 Trunk partition.

Fig. 6 Interconnection requirement D' .

grids. Consider the requirement D' which results from the insertion of $N-1$ non-terminal grids between every pair of adjacent vertical grids for the requirement D .

$$D' = [T_1', T_2', \dots, T_N', L, R]$$

$$T_1' = (\underbrace{0, \dots, 0}_{N-1}, \underbrace{t_{i1}, 0, \dots, 0}_{N-1}, \underbrace{t_{i2}, \dots, t_{iP-1}, 0, \dots, 0}_{N-1}, t_{iP})$$

Let T_2' be the ordered alignment of terminals. T_2' is defined by

$$T_2' = (t_{N1}, t_{N-11}, \dots, t_{21}, 0, t_{N2}, t_{N-12}, \dots, t_{22}, 0, \dots, t_{NP}, t_{N-1P}, \dots, t_{2P}, 0)$$

Consider the requirement $[T_1', T_2', L, R]$ of two cell-rows. Let C_{NM}' be the maximum number of the crossing nets for the requirement $[T_1', T_2', L, R]$. C_{NM} and C_{NM}' are related by $C_{NM}' \leq C_{NM}$. For terminals $t_{Nj}, t_{N-1j}, \dots, t_{2j}, 0$ in T_2' , it is not necessary that the alignment order is $t_{Nj}, t_{N-1j}, \dots, t_{2j}, 0$. Then, $C_{NM}' = C_{NM}$ if and only if $|C_N(j) \cap C_N(j+1)| = C_{NM}$ for a j ($1 \leq j \leq P-1$). Since there are no vertical constraints^{1,2} for the requirement $[T_1', T_2', L, R]$, the possible minimum width is C_{NM}' , and then no trunk partitions need be introduced into the nets (i.e. each net consists of a single horizontal segment)^{1,2}. Therefore, for the requirement $[T_1', T_2', L, R]$, the routing is completed by using at most C_{NM} horizontal grids and then no trunk partitions need be introduced into the nets.

Next, the problem of routing nets interconnecting two terminals of each number t_{ij} in T_2' and T_1' ($2 \leq i \leq N$), given in Fig.6, is considered. The routing can be completed by using $N-1$ horizontal grids as shown in Fig.6.

Combining the two routing as shown in Fig.6, the whole routing is obtained for the requirement D' . Thus, for the requirement D , the routing which satisfies the restriction imposed on the number of trunk partitions can be completed by using at most $C_{NM}+N-1$ horizontal grids. (Q.E.D.)

Consider the requirement D'' which results from the insertion of N non-terminal grids between every pair of adjacent vertical grids for the requirement D . If, for the requirement D'' , we follow the procedure similar to the proof of Theorem 2 to complete the routing by using $C_{NM}+N$ horizontal grids, we can transfer the horizontal wire segments assigned to the one same horizontal grid in the first horizontal channel into the other channel as shown in Fig.7. Thus the following theorem holds.

[THEOREM 3] The number of trunk partitions is restricted as shown in Theorem 2. If at most $C_{NM}+N$ horizontal grids are available for a given requirement D , the routing can be completed regardless of the number of available horizontal grids in each horizontal channel. (END)

The number of trunk partitions is restricted

Fig. 7 Transferring of horizontal wire segments.

as shown in Theorem 2. Then, for a given requirement D , it has been proved that the minimum number G of horizontal grids used in the routing satisfies

$$C_{TM} \leq G \leq C_{NM} + N - 1 \quad (7)$$

(where the possible minimum width given in Theorem 1 is less than $C_{NM} + N - 1$ by Lemma 1 and the necessary and sufficient condition⁴ for the possible minimum width to be $C_{TM} + 1$). It has been proved that the routing can be completed regardless of the number of available horizontal grids in each horizontal channel when $C_{NM} + N$ horizontal grids are available.

The remainder of this section will be devoted to the discussion on how many non-terminal grids inserted are sufficient to complete the routing shown in Theorem 3. As mentioned in the section 2, in actual cases the insertion of non-terminal grids is not permitted, but non-terminal grids has been prepared so that vertical wirings are possible on the grids. Furthermore, vertical grids corresponding to unused terminals can be used for vertical routings. In the masterslice LSI considered, most of the nets consist of the nets interconnecting terminals in the one same cell-row and the nets interconnecting terminals in the two adjacent cell-rows. For a given requirement D , we accordingly suppose that all the nets consist of the one-row nets and the two-row nets defined later.

The one-row net is defined as the net to interconnect only the terminals in the one same cell-row. The two-row net is defined as the net to interconnect only the terminals in the two adjacent cell-rows. Fig.8 shows such nets. We suppose that the one-row net is routed in the lower horizontal channel adjacent to the cell-row to which the net is connected and that the two-row net is routed in the horizontal channel between the two cell-rows to which the net is connected as shown in Fig.8. In particular, we suppose that the one-row net to interconnect the terminals in the N th cell-row is routed in the $(N-1)$ th horizontal channel.

[DEFINITION 4] For a given requirement D each net is assigned to a horizontal channel and is routed in it. Then, $C_N^i(j)$ is the set of all nets that satisfy the following two conditions.

Fig. 8 One-row net and two-row net.

Fig. 9 Detour of wire route.

- (1) The nets are assigned to the i th horizontal channel.
- (2) The nets cross the vertical grid v_j at least once in any routing or terminate at a terminal on the vertical grid v_j .

The maximum crossing number C_{NM}^i of the i th horizontal channel is defined as follows.

$$C_{NM}^i = \max_{1 \leq j \leq P} |C_N^i(j)| \quad (8)$$

(END)

C_{NM} and C_{NM}^i are related by

$$C_{NM} \leq \sum_{i=1}^{N-1} C_{NM}^i \quad (9)$$

In the remainder of this section, $\sum_{i=1}^{N-1} C_{NM}^i$ is written as ΣC_{NM}^i , for notational simplicity.

Case 1: $C_{NM} = \Sigma C_{NM}^i$. For a given requirement D , the whole routing will be obtained by combining the routed horizontal channel between two adjacent cell-rows. By Theorem 2, we can route the i th horizontal channel using $C_{NM}^i + 1$ horizontal grids. Thus the following theorem holds.

[THEOREM 4] For a given requirement D , we suppose that all the nets consist of the one-row nets and the two-row nets and $C_{NM} = \Sigma C_{NM}^i$. The number of trunk partitions is restricted as shown in Theorem 2. If at most $C_{NM} + N - 1$ horizontal grids are available, the insertion of a non-terminal grid between every pair of adjacent vertical grids is sufficient to complete the routing. (END)

Case 2: $C_{NM} < \sum C_{NM}^i$. If the routes of a set of nets are detoured so as to satisfy the equation $C_{NM} = \sum C_{NM}^i$ as shown in Fig.9, the routing which satisfies the constraint of the number of trunk partitions in Theorem 2 is completed by using at most $C_{NM} + N$ horizontal grids. (Let the set of the nets be Q .) This fact is guaranteed by Theorem 3. For example, the net shown in Fig.9(ii) is assigned to the i th horizontal channel. Here, it is sufficient that the number of inserted non-terminal grids is q more than that of the former case, where

$$q = \sum_{W_i \in Q} [\text{number of terminals interconnected by the net } W_i] \quad (10)$$

5. Experimental Results and Discussion

This section describes the experimental results of a masterslice LSI circuit with 624 gate cells. It is shown that the number of horizontal grids used in the routing by the routing program is approximately $C_{NM} + N$ as shown in Theorem 3 and Theorem 4.

5.1 Chip Structure and Outline of Routing Program

The whole structure of the masterslice LSI chip used in the experiment is shown in Fig.1, where arranged are 14 cell-rows (i.e. $N=14$) and 13 horizontal channels for routing. The metal interconnections are made on two layers. 624 gate cells are arranged in the rows. A set of 52 gate cells and 74 feed-through cells each of which can be used for one vertical wiring is arranged in each cell-row as shown in Fig.10. In particular, input and output buffer cells are arranged in the first cell-row and the 14th cell-row. The aluminum conductor for power supply penetrates the cell-rows as shown in Fig.10. As is shown in Fig.11, the gate cell has the logic function of 3-input NOR gate and pairs of electrically equivalent connection points at which nets can be connected to gate cell terminals are prepared on both top and bottom sides of each gate cell. When a gate cell is unused as a logic gate or is used either as an inverter or a 2-input NOR gate, it has unused terminals so that vertical wirings are possible on the vertical grids corresponding to these unused terminals.

The routing program⁸⁻¹⁰ used in the experiment is developed as the routing subsystem of a computer aided layout system, MARS-MIII⁹, for this masterslice LSI chip. The processing flow of the routing program is outlined in Fig.12. The algorithm used here is an improved version of the routing algorithm

with two stages of global and channel routings⁷. The improvement is found in the introduction of the net-transferring⁸ which can be effectively done due to the characteristic that gate cell terminals can be connected with nets from above and below. The first phase of the routing is the global routing and the procedure is as follows: Each net is assigned to one or more channels depending upon the pseudo Steiner tree in the network with the edges corresponding to the channels and the feed-through cells and with the vertices corresponding to the boundaries between a channel and a feed-through cell. After the global routing, the terminal assignment and the channel routing based on the improved dogleg algorithm are carried out in the channel order, starting at the lowest horizontal channel. The function of the terminal assignment is to interchange logically equivalent gate cell terminals so that the vertical constraints and each trunk length are minimized as possible. If a cyclical constraint occurs in the vertical constraint graph^{1,2}, one trunk is divided into two or more trunks in order to eliminate the cyclical constraint in the channel routing step. The channel routing step determines the precise wire route of each net in the horizontal channel. If the number of required horizontal grids exceeds the number of horizontal grids in the processed channel, the routing modification is carried out by transferring one-row nets into the upper channel as shown in Fig.13.

5.2 Experimental Results and Discussion

Table 1 shows the routing results which have been achieved using this routing program in MARS-MIII for the case of the masterslice LSI with 624 gate cells. In this case, the automated placement program^{9,11} in MARS-MIII was also used.

As is shown in Table 1, the number of horizontal grids required by this routing program is more than $C_{NM} + N$. By studying the routing results, it is found due to the following inefficiency of this routing program.

- (i) The global routing and the net-transferring are not effectively carried out in order to relieve local wiring congestion and to route all of the nets in the fewest possible number of horizontal grids.
- (ii) If there are no cyclical constraints in the vertical constraint graph, in the channel routing step trunk partitions will only be introduced at a terminal position for the nets (i.e. n -terminal nets have at most $n-2$ sites for trunk partitions).

Fig. 10 Arrangement of gate cells in a cell-row.

Fig. 11 Gate cell.

Fig. 12 Processing flow of the routing program.

Fig. 13 An example of net-transferring.

The number of horizontal grids used in the resultant routing is approximately $C_{NM}+N$ as shown in Table 1, when each routing result of this program is modified manually with the following four tactics.

- (1) Transfer a one-row net. (See Fig.13.)
- (2) Divide one trunk into two or more trunks. (See Fig.5.)
- (3) Detour the route of a net. (See Fig.9.)
- (4) Modify the detoured route of a net. (See Fig.9.)

Fig.14 shows the routing result modified manually for circuit A in Table 1. As is clear from Table 1, the number of horizontal grids used in the routing modified manually, as well as that in the routing by this program is much more than the minimum width C_{TM} or $C_{TM}+1$. If, for a given requirement D, the conditions of Theorem 4 is satisfied, it is anticipated that the assignment of the nets to horizontal channels carried out by this program will be almost the same as in Theorem 4 and that this program will be able to accomplish the routing in $C_{NM}+N-1$ horizontal grids with some manual modifications. Here, as shown in Table 1, most of the nets are one-row nets and two-row nets. If a non-terminal grid is inserted between every pair of adjacent vertical grids, it is anticipated by Theorem 3 and Theorem 4 that this program will be able to accomplish each routing in $C_{NM}+N$ horizontal grids with some manual modifications. This insertion of non-terminal grids can, in effect, be

Table 1, Experimental results.

Circuit	A	B	C	D
S (=No. of nets)	585	618	576	566
$([\text{No. of one-row nets}] + [\text{No. of two-row nets}])/S$	83%	84%	83%	84%
No. of unroutable nets	1	1	0	0
No. of used terminals*	1794	1958	1773	1749
No. of unused terminals*	1590	1426	1611	1635
No. of terminals which are unused as logic terminals and used for vertical routings	359	482	361	351
C_{NM}	99	118	106	102
C_{TM}	99	118	107	102
$C_{NM}+N$	113	132	120	116
No. of horizontal grids used in routing by routing program	121	139	124	119
No. of nets modified manually	16	19	20	13
No. of horizontal grids used in routing modified manually**	113	131	119	114

*Number of used (unused) terminals is $\sum_{i=2}^{N-1} [\text{number of used (unused) gate cell terminals in the } i\text{th cell-row}]$ where a feed-through cell counts as a unused terminals.

**Unroutable nets were routed manually.

considered nearly equivalent to the occurrence of unused terminals, the number of which is just the number of the terminals used as logic terminals. Since the number of the unused terminals is nearly equal to that of the terminals used as logic terminals, it is considered that each routing has been completed in $C_{NM}+N$ horizontal grids using this routing program with some manual modifications as shown in Table 1.

Most of the nets in the masterslice LSI considered are one-row nets and two-row nets as shown in Table 1, when the optimal placement is determined with respect to minimal wire length. The experimental results lead to the following conclusion: If, for a given requirement D, the number of unused terminals is nearly equal to that of the terminals used as logic terminals, it can be predicted that the number of horizontal grids used in the routing by the general routing program will be approximately $C_{NM}+N$ as shown in Theorem 3 and Theorem 4.

Fig. 14 Routing result with manual modifications for circuit A in table 1.

6. Conclusion

For a given requirement D, a number of trunk partitions must often be introduced in order to complete the routing by the minimum width. Hence, the general routing program will be unable to complete the required routing by the minimum width. In this paper, when the number of trunk partitions is restricted in that n -terminal nets have at most n sites for trunk partitions, it has been proved that the minimum number G of horizontal grids used in the routing satisfies

$$C_{TM} \leq G \leq C_{NM} + N - 1 \quad (11)$$

Furthermore, when $C_{NM} + N$ horizontal grids are available, it has been proved that the routing can be completed regardless of the number of available horizontal grids in each horizontal channel.

The experimental results are shown for the masterslice LSI with 624 gate cells. Most of the nets in the masterslice LSI considered are one-row nets and two-row nets, when the optimal placement is determined with respect to minimal wire length. The experimental results lead to the following conclusion: If, for a given requirement D, the number of unused terminals is nearly equal to that of the terminals used as logic terminals, it can be predicted that the number of horizontal grids used in the routing by the general routing program will be approximately $C_{NM} + N$. By employing this conclusion, if the terminal assignment step is initially carried out in the routing program, it is possible to predict whether or not the required routing will be completed after the terminal assignment step, and the occurrence of unroutable nets will be greatly reduced.

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